HARDWARE
REFERENCE

ENP-2611

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RadiSys
THE POWER OF WE

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Before you begin

This guide describes the RadiSys ENP-2611, a board that contains the Intel† IXP2400 network processor (IXP2400), a high-speed packet-processing chip.

The guide describes the board's main components and layout. It also explains how to install and configure the ENP-2611.

Book/File
For information about the ENP Software Development Kit that accompanies this board, see the *ENP SDK Programmer's Guide*.

The ENP-2611 is for:

- Application developers that create and deploy network applications that require sophisticated packet manipulation.
- Network equipment vendors and original equipment manufacturers that want to integrate the architecture into a variety of network equipment devices.

Examples of typical network applications include:

- Security applications, including firewalls and intrusion detection.
- Bandwidth and traffic management applications, including server load balancing and quality of service.
- Network monitoring and management applications, including remote monitoring and service level management.
- Routers and switches.

About this guide

Contents

Chapter/appendix		Description
1	Overview	Introduces the ENP-2611, briefly describes its features, and lists specifications.
2	Installation and configuration	Describes how to install an ENP-2611 in a Windows NT workstation.
3	Theory of Operation	Provides information about the ENP-2611's layout and main components.
A	IXP2400 Memory Map	Lists the IXP2400's major sections.

Chapter/appendix		Description
B	Registers	Describes those configuration registers on the IXP2400 that are unique to the ENP-2611.
C	Connectors	Details the location, function, and pin-outs of the ENP-2611's connectors, jumpers, and LEDs.
D	SPI-3 Bridge register definitions	Defines the SPI Bridge registers.

Notational conventions

This manual uses the following conventions:

- `Screen text and syntax strings appear in this font.`
- All numbers are decimal unless otherwise stated.
- Bit 0 is the low-order bit. If a bit is set to 1, the associated description is true unless otherwise stated.

Notes indicate important information about the product.

Tips indicate alternate techniques or procedures that you can use to save time or better understand the product.

The globe indicates a World Wide Web address.

The book indicates a book or file.

ESD cautions indicate situations that *may* cause damage to hardware via electro-static discharge (ESD).

Cautions indicate potentially hazardous situations which, if not avoided, may result in minor or moderate injury, or damage to data or hardware. It may also alert you about unsafe practices.

Warnings indicate potentially hazardous situations which, if not avoided, can result in death or serious injury.

Danger indicates imminently hazardous situations which, if not avoided, will result in death or serious injury.

Where to get more information

About the ENP-2611

You can find out more about ENP-2611 from these sources:

- World Wide Web: RadiSys maintains an active site on the World Wide Web. The site contains current information about the company and locations of sales offices, new and existing products, contacts for sales, service, and technical support information. You can also send e-mail to RadiSys using the web site.

Note

When sending e-mail for technical support, please include information about both the hardware and software, plus a detailed description of the problem, including how to reproduce it.

URL

To access the RadiSys web site, enter this URL in your web browser:

`http://www.radisys.com`

Requests for sales, service, and technical support information receive prompt response.

- Other: If you purchased your RadiSys product from a third-party vendor, you can contact that vendor for service and support.

About related RadiSys products

ENP SDK (Software Development Kit)

The ENP SDK provides programming methodology, tools, and runtime libraries that you use to quickly develop optimized, multi-algorithm, multi-channel applications for the Intel† IXP-2400 chip.

Other

ENP-2611 components

For additional information about some ENP-2611 components, see the following documents located on the Intel IXA (Internet Exchange Architecture) SDK CD-ROM:

- *IXP2400 Network Processor Data Sheet*
- *IXP2400 Hardware Reference Manual*

URL
The following web site provides additional information about the board's main components: http://developer.intel.com

Wind River Tornado

These documents are part of the document set provided when you purchase Tornado:

Tornado User's Guide, Explains how to use Tornado, an integrated StrongARM development environment from Wind River.

Tornado API Programmer's Guide and VxWorks Programmer's Guide, Explains how to modify VxWorks source code.

PCI architecture

PCI System Architecture, Fourth Edition, published by Addison-Wesley and authored by Mindshare, Inc.

PCI specifications, available at the PCI SIG web site:

URL
www.pcisig.com

Other

Intel® Sausalito Network Processor Customer Information Book Volume 1 Rev. 0.4 #11894. Intel, June 2002

Intel® Sausalito Network Processor Customer Information Book Volume 2 Rev. 0.4 #11895. Intel, June 2002

Intel® IXP2400 Network Processor Hardware Reference Manual. Intel, January 2003

Intel® IXP2400 Network Processor Datasheet. Intel, April 2003

Intel® IXP2400 Network Processor Specification Update. Intel, March 2003

PCI Local Bus Specification, Revision 2.3. PCI Special Interest Group, March 29, 2002

21555 Non-Transparent PCI/PCI Bridge User Manual, #278321-002 Intel, July 2001

PCI2050/PCI2050I PCI-to-PCI Bridge Data Manual, SCPS053A Texas Instruments, 2000

PCI2050B PCI-to-PCI Bridge Datasheet, SCPS076 Texas Instruments, February 2003

PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification Revision 1.0 JEDEC, March 4, 2001

PM3386 S/UNI-2XGE Dual Gigabit Ethernet Controller Datasheet Issue 7, PMC-Sierra, July, 2001

PM3386 S/UNI-2XGE Dual Gigabit Ethernet Controller Reference Design Issue 3, PMC-Sierra, September, 2001

PM3387 S/UNI-1XGE Gigabit Ethernet Controller Datasheet Issue 2, PMC-Sierra, September 2002

Small Form Factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA), September 14, 2000

V23828-K305-P57 Small Form Factor Pluggable SFP Multimode 850nm 2.125 and 1.0625 Gbits/s FibreChannel, 1.25 Gigabit Ethernet Transceiver with LC Connector, PCI Height Variant, Infineon Technologies, July 21, 2003

3.3V SFP LC Transceiver for Fibre Channel & 1000Base-SX, E2O Communications, April 15, 2002

74741-0002 SFP 1000Base-T RJ-45 Gigabit Ethernet Copper Transceiver, Molex, September 2003

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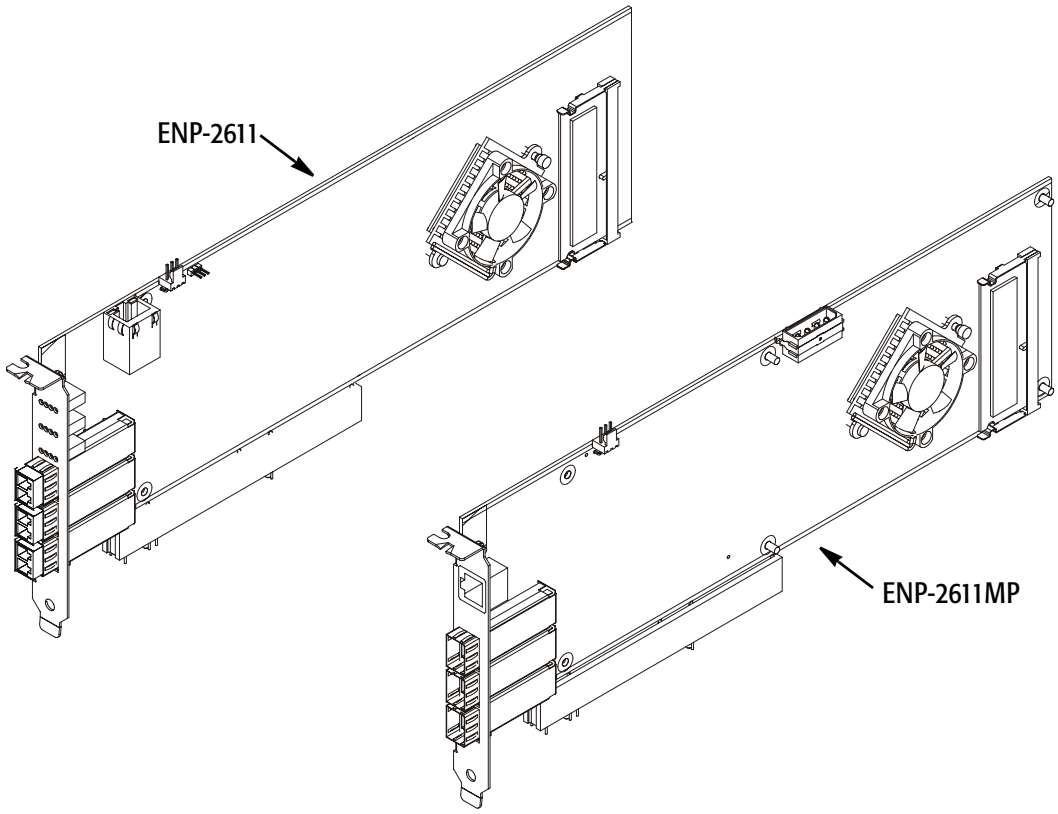
1 Overview

This document specifies the ENP-2611, a Network Processor board based on the IXP2400 and implemented as a full-length PCI adapter form factor.

Figure 1-1. The ENP-2611 boards



The ENP-2611 can be ordered in these configurations:

> **Note**
> Before ordering, go to www.radisys.com to confirm the availability of the product configuration(s) you want.

Table 1-1. ENP-2611 configurations

Configuration	Description
ENP2611-256	IXP2400, 600Mhz, 256MB DDR SDRAM, 8MB QDR SRAM.
ENP2611-512	IXP2400, 600Mhz, 256MB DDR SDRAM, 16MB QDR SRAM.
ENP2611-256-C	IXP2400,600MHz,256MB DDR SDRAM,8MB QDR SRAM, Copper interface.
ENP2611-512-16-C	IXP2400,600MHz,512MB DDR SDRAM,16MB QDR SRAM,Copper interface
ENP2611MP-256	IXP2400,600MHz,256MB DDR SDRAM,8MB QDR SRAM, Fiber interface with MP.
ENP2611MP-256-C	IXP2400,600MHz,256MB DDR SDRAM,8MB QDR SRAM, Copper interface w/MP[1].
ENP2611MP-512-16	IXP2400,600MHz,512MB DDR SDRAM,16MB QDR SRAM,Fiber interface w/MP[1].
ENP2611MP-512-16C	IXP2400,600MHz,512MB DDR SDRAM,16MB QDR SRAM,Copper interface with MP[1].

[1] MP (Management Port) configurations include a debug Ethernet connector on the rear panel.

The ENP-2611 requires a backplane that supports the *CompactPCI Specification Revision 2.1*.

Features

The ENP-2611. based on an Intel IXP2400 network processor, includes these features:

- IXP2400 Processor running at 600 MHz, consisting of the following blocks:
  - One 32-bit X-Scale RISC processor compatible with the ARM Version 5 architecture. The X-Scale initializes and manages the chip, and performs higher-layer network processing tasks.
  - Eight 32-bit programmable Microengines specialized for network processing. They do the main data plane processing per packet.
  - Single-channel DDR SDRAM Controller with ECC. DRAM is typically used for data buffer storage.
  - Two independent QDR SRAM Controllers. SRAM is typically used for control information storage.
  - 16KB Scratchpad Memory for general-purpose use.
  - MSF (Media and Switch Fabric interface). This is the interface for network framers and/or switch fabric. It contains transmit and receive buffers.
  - Hash Unit. The X-Scale and Microengines can use this to offload hash calculations.

    - 64-bit Rev 2.2 PCI Controller.
    - Chip-wide control and status registers (CAP). These provide interprocessor communication features.
    - X-Scale Peripheral Interface (XPI). This consists of the Interrupt Controller, Timers, UART, General-purpose I/O (GPIO), and Slow Port Interface to off-chip peripherals.
    - Performance Monitor. These counters can be programmed to count internal hardware events to analyze and tune performance.
- Up to 1GB of +2.5V DDR ECC SDRAM in a single 200-pin SODIMM socket. Modules must be 1.25" high maximum. Currently, 256MB and 512MB ECC modules are supported.
- One or two 2Mx18 QDR II (1.8V) SRAMs on each of the two QDR channels, for a total of 8MB (one per channel) or 16MB (two per channel).
- 16MB of StrataFlash memory to store boot code.
- SPI-3 Bridge FPGA.
    - Connects directly to the IXP2400 MSF interface running in POS-PHY Level 3 (aka SPI-3) mode.
    - Provides connection and data routing from the IXP2400 to a PM3386/7 Gigabit Ethernet MACs.
- One PM3386 Dual Gigabit Ethernet Controller that provides two interfaces.
    - Connected via SPI-3 interface directly to the “PHY0” port of the FPGA SPI-3 Bridge.
    - Internal SERDES are connected to two transceiver modules.
    - Tranceivers conform to SFP (Small-Form-factor-Pluggable) MSA (Multi-Source Agreement), modified for PCI applications.
- One PM3387 Gigabit Ethernet Controller providing one interface.
    - Connected via SPI-3 interface through Option Board connector to the “PHY1” port of the FPGA SPI-3 Bridge.
    - Internal SERDES are connected to one transceiver module.
    - Tranceiver conforms to SFP (Small-Form-factor-Pluggable) MSA (Multi-Source Agreement), modified for PCI applications.
- Intel 21555 non-transparent PCI-to-PCI bridge connecting the internal 64-bit PCI bus to the backplane Host PCI Bus.
    - Bus-master access from the IXP2400 to devices on the backplane Host PCI bus.
    - Access from the Host processor to onboard devices, DDR DRAM, and QDR SRAM.
    - Doorbell registers to provide inter-processor interrupts.
    - Scratchpad registers to provide inter-processor communication between the Host and the IXP2400.

- TI PCI2050B transparent PCI-to-PCI bridge connecting the internal 64-bit PCI bus to a downstream 32-bit PCI Bus.
- Intel 82559 PCI Ethernet controller.
  - Connected to the 21150 downstream Local32 PCI bus.
  - Supports 10BaseT or 100BaseTX via onboard RJ45 connector.
- SPI-3 Option Board connector:
  - Connected to the 21150 downstream Local32 PCI bus.
  - Provides future expansion opportunity.
- Clock generation circuitry:
  - IXP2400 System Clock.
  - IXP2400 MSF/FPGA Interface Clock.
  - FPGA/PM338x Interface Clock.
- Reset and initialization circuitry.
- Power:
  - +1.3V IXP2400 Core supply.
  - +2.5V and +1.25V DDR SDRAM supply.
  - +1.5V and 0.75V QDR SRAM supply.
  - +1.8V supply.
  - Power supply sequencing.

External Interfaces

Note

For detailed information about LEDs, see *Indicator LEDs* on page 59.

The ENP-2611 provides the following I/O connectors:

- Three shielded SFP LC optical fiber or copper transceivers accessible on the front bracket.
- Three Quad-stacked LEDs that provide the following indicators (on the front bracket of only the non-MP version):
  - One yellow “Transmitter Disabled” status for each gigabit Ethernet channel.
  - One yellow “Transmitter Fault” status for each gigabit Ethernet channel.
  - One green “Loss of Signal” status for each gigabit Ethernet channel.
  - One green software-controlled “USER” status for each gigabit Ethernet channel.

  The Management Port (MP) version has one shielded RJ45 connector with built-in LEDs for 10/100BaseT Debug Ethernet interface accessible on the front bracket. This version has no LEDs for the Gigabit ethernet channels.
- Universal 64-bit PCI bus edge-card connector.

Internal Interfaces

The ENP-2611 provides the following I/O connectors internal to the board:

- The non-MP version of the product has one shielded RJ45 connector with built-in LEDs for 10/100BaseT Debug Ethernet interface on the top edge of the board.
- One 10x40 0.050" pitch shrouded connector to allow attachment of a future SPI-3 Option Board, containing:
  - 32-bit SPI-3 bus with input and output pins per signal.
  - 32-bit 33 MHz PCI bus for maintenance and programming.
  - Non-multiplexed Slow Port bus for programming.
- One 3-pin 1x3 0.100" pitch right-angle shrouded connector for serial interface on the top edge of the board.
- One 2-pin 1x2 0.100" pitch straight right-angle connector for IXP2400 fan/heatsink.
- Manufacturing connectors for self-test, burn-in, and configuration.

Socketed Options

Either a 256MB or 512MB DDR SDRAM module is installed.

Accessories

Female DB-9 to female 3-pin header null-modem Debug Serial Cable (RadiSys part number 044-00612-0000).

Environmental Specifications

The ENP-2611 meets the following environmental specifications. The ESD, EMC, and Immunity specifications are measured only under ambient temperature and humidity (at any point between 20° C to 30° C and humidity at any point between 30% to 50%).

Note

Because any meaningful emissions agency certification must include the entire system, RadiSys does not provide environmental certification testing. The ENP-2611 is designed and tested to pass the environmental specifications noted below as “designed and tested, but not certified”.

In addition, the operating environment must provide sufficient airflow across the board to keep it within its temperature specification.

Table 1-2. Environmental Specifications

Characteristic	State	Value
Temperature (ambient)	Operating	0° C to +50° C (over processor)[1]. Operation above +50° C reduces the maximum operational relative humidity.
	Storage	–40° C to +70° C, 5° C per minute maximum excursion gradient.
Airflow	Minimum	60 LFM
Relative humidity	Operating	10% to 85% RH non-condensing at +30º C, linearly decreasing to 5% to 15.5% RH non-condensing at +65º C.
	Storage	5% to 90% RH non-condensing at +40º C.
Shock[2]	Unpackaged	**GR-63-CORE, R4-45** Drop on 1 face, 2 edges, 2 corners per above.
	Packaged	**GR-63-CORE, Category A, R4-43** Drop on 3 faces, 3 edges, 4 corners per above.
Vibration[2]	Operating	**GR-63-CORE, R4-58 and R4-59** Swept sine, 5–100–5Hz, 0.1g, 0.1 octaves/min, 3 axes.
	Storage	**GR-63-CORE, R4-60 (curve 2)** Swept sine, 5–50Hz, 0.5g, 0.1 octaves/min, 3 axes. Swept sine, 5–50Hz, 3.0g, 0.2 octaves/min, 3 axes.
MTBF		Calculated 400,000 hours at 30° C using Bellcore Issue 6.
Power consumption	Maximum	3.1A @ +5V 2.5A @ +3.3V 0.1A @ +12V

1 Derated 2° C per 1000 feet (300 meters) over 6600 ft (2000 meters) with sufficient airflow to keep within the temperature specification.

2 The ENP-2611 conforms to the shock and vibration requirements contained in NEBS document GR-63.

Table 1-3. Physical Specifications[1]

Characteristic	Value
Dimensions	Full-length 64-bit Universal PCI adapter board (approximately 4.1" x 12.3").
Board thickness	0.063" (1.6mm).
Component height[2] Primary side Secondary side	 0.570" (14.48mm) 0.105" (2.67mm)

1 Per PCI Local Bus Specification, revision 2.1 or 2.2.

2 This board contains Z-axis violations due to the following:

- The height of the Ethernet RJ45 connector. The RJ45 connector has an integral pulse transformer and LEDs which slightly exceed the primary-side height requirement of 0.570".
- The BGA connector for the Option Board on the secondary side. The PCI component height specification is 0.105" on the board's secondary side. The connector with its mating shorting board extends a total of 0.285" above the surface of the board's secondary side. This intrudes slightly (0.055") into the primary component height area of the board located in the adjacent slot behind

this board.

Table 1-4. Immunity and Emissions

Characteristic	State	Value
ESD	Operating	(All performance criteria from EN61000-4-2:1995)[1] 4KV direct contact, performance criteria B 6KV direct contact, performance criteria C 4KV air discharge, performance criteria B 8KV air discharge, performance criteria C
Fast tranisient/burst	Operating	EN61000-4-4:1995, performance criteria B[1]
Surge voltages	Operating	EN61000-4-5:1995, performance criteria B[1]
Conducted immunity	Operating	EN61000-4-6:1995, performance criteria A[1]
Radiated immunity 3 V/m test level	Operating	EN61000-4-3:1995, performance criteria A[1]
Radiated & Conducted Emissions (EMC)	Operating	EN55022:1998, Class A[1]
Product safety		Designed to meet the requirements of EN60950/UP60950[1]

[1] These are system level tests. This board is designed and certified to pass in the RadiSys 7581 4U ATX Server Chassis. When installed in other systems, the system's performance affects this board's ability to conform to these specifications. Agency testing and certification must be completed on other systems.

2 Installation and configuration

This chapter describes how to install an ENP-2611 reference board in a Windows workstation.

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The ENP-2611 includes one 4-position (SW2) DIP switch for user configuration:	10
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Note

This PCI card is for use only with compatible UL listed ITE equipment that have installation instructions detailing user installation of card cage accessories

ESD WARNING

Avoid causing ESD (electrostatic discharge) damage:

- Keep the card in its anti-static bag until you are ready to install.
- Install the card (as described later in this chapter) only in a static-free environment:
  - Wear an antistatic wrist strap attached to a known ground such as an antistatic lab mat.
  - Remove the card from its antistatic bag only in a static-free environment.
  - Avoid touching printed circuits, connector pins, and components. Where possible, hold the card only by its edges or mounting hardware.
  - Make the least possible movement with your body to minimize electrostatic charges created by contact with clothing fibers, carpet, and furniture.
  - Keep one hand on the computer chassis, if possible, as you insert or remove a card.
  - Avoid placing the card on the chassis cover or on a metal table. The cover and metal table increase the risk of damage because they provide an electrical path from your body through the card.
- Always turn the computer off before removing a card from the chassis.

The ENP-2611, like most other electronic devices, is susceptible to ESD damage. ESD damage is not always immediately obvious. It can cause a partial breakdown in semiconductor devices that might not result in immediate failure.

Before you begin

The ENP-2611 requires the following:

- Adequate ventilation, as described in Table 1-2: *Environmental Specifications* on page 6.
- A PC that runs Windows 2000.
- The serial cable that comes with the ENP-2611. (The cable connects the serial port on the board to the Windows workstation.)

  For a description of the serial cable, including pin information, see *Null-modem serial cable* on page 61.
- Software:
  - Internet Exchange Architecture (IXA) Software Developers Kit version 1.3 (1.3.141) or 2.0 (2.0.83) for the Windows workstation, and the version 1.3A patch for the Windows workstation. This is an integrated development VxWorks environment for developing and delivering code targeted for microengines.
  - Tornado 2.0, available from Wind River Systems, Inc., for StrongARM† development.
  - ENP SDK 2.0. The ENP SDK supports VXworks version 5.4.

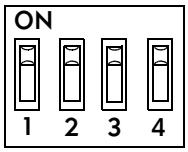
Setting jumpers and switches

DIP switches

The ENP-2611 includes one 4-position (SW2) DIP switch for user configuration:

Figure 2-1. ENP-2611 DIP switch: default settings

ON = Switch closed
OFF = Switch open



SW2

Table 2-1. SW2 DIP switch settings

Switches	Value		Description
1 and 2	0, 0	On, On	Sets DRAM window size to 128MB.
	0, 1	On, Off	Sets DRAM window size to 256MB.
	1, 0	Off, On	Sets DRAM window size to 512MB.
	1, 1	Off, Off	Sets DRAM window size to 1024MB (default).
3 and 4	0, 0	On, On	Sets SRAM window size to 8MB.
	0, 1	On, Off	Sets SRAM window size to 16MB.
	1, 0	Off, On	Sets SRAM window size to 32MB.
	1, 1	Off, Off	Sets SRAM window size to 64MB (default).

Installing the ENP-2611

To install the ENP-2611 in your Windows workstation:

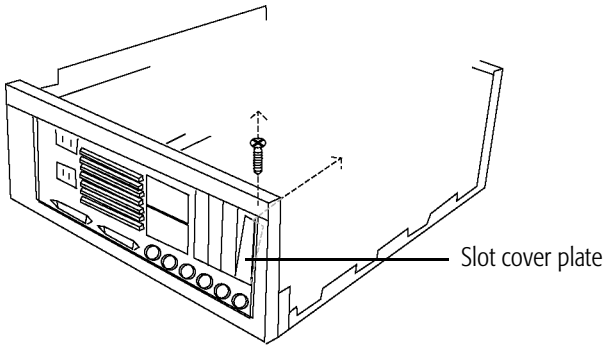
1. Remove the ENP-2611 from the packaging:
   A. Remove the ENP-2611 from its antistatic bag.
   B. Check the ENP-2611 for any visible signs of damage.

Note
Leave all DIP switches in the default (OFF) position.

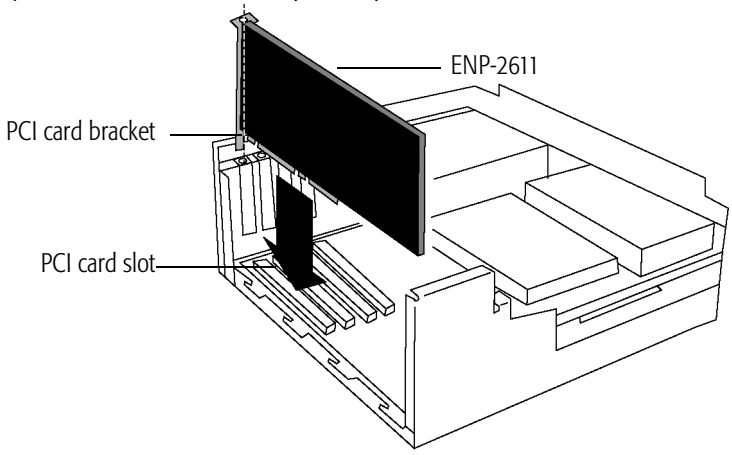
2. Install the board:
   A. Select a PCI card slot in which to install the ENP-2611.

Note
• The ENP-2611 must be installed in a PCI slot that supports bus mastering. Most PCI slots in most systems do; however, a few do not. Check with the motherboard manufacturer. • The PCI slot must provide both +3.3V and +5V voltages.

   B. Remove the screw that secures the slot's cover plate to the rear panel of the PC, and remove the cover plate.



   C. Remove any installed SFP transceivers.
   D. Line up the ENP-2611 visually with your PCI card slot as shown:



E. Slide the flat outside edge of the board under the bracket closest to the system board and align the PCI card bracket with the card support on the rear panel of the PC.

F. Insert the ENP-2611 into the PCI card slot and push firmly to seat the board in the slot.

G. Secure the board to the PC with the screw you removed in step 2B.

H. Re-install removed SFP transceivers

I. Replace the PC's cover following the manufacturer's instructions.

3. Connect the custom serial cable shown in the figure in *Debug Serial Port Header* on page 61.
4. Connect the Ethernet cable to the RJ45 connector as shown in *Debug Ethernet connector* on page 60.
5. Connect all other peripherals to the PC and connect it to a power source.

Using the Boot Manager

The ENP Software Development Kit (SDK) includes the Boot Manager. From this application you can execute other available boot options.

To select a boot option:

1. Set your COM port to:

Baud rate:	57600
Parity:	N (no parity)
Data bits:	8
Stop bits:	1
Flow control:	N (no flow control)

2. Power on the ENP-2611. The Boot Manager starts and displays this on the serial port:

   ```
   Redboot>
   ```

   You can specify which application executes at boot by using the BootManager's fconfig command. For detailed information about the Boot Manager and its commands, see *Configuring the ENP board for boot* the in *Chapter 2, Installation and configuration* in the *ENP SDK Programmer's Reference*.

Post-installation troubleshooting

You can use the diagnostics and System Monitor that come with the ENP Software Development Kit to diagnose and correct hardware problems in the ENP-2611. For a description of these diagnostic tools, see the *ENP SDK Programmer's Reference*.

In addition, the next table lists symptoms and possible solutions to some hardware problems that might occur after you install the ENP-2611.

Table 2-2. Post-installation troubleshooting

Symptom	Possible solutions
The PC does not recognize a PCI card in the ENP-2611 slot.	Ensure that the ENP-2611 board, memory, and cable are properly installed. Ensure that the ENP-2611 is functioning by using the debug port to watch for serial output. If the PC still does not recognize the ENP-2611, use the diagnostics provided with Windows.
The PC does see a PCI card in the ENP-2611 slot, but does not recognize it as an ENP-2611.	Ensure that the workbench was successfully installed on the host PC.
Your system boots, but takes a long time to do so.	This is normal operation. When the operating system initializes, it must reset the Primary Access Lockout Bit in the 21555, allowing the CPU controller to read configuration information. In some cases, this can take twenty seconds or more.
Your PC does not receive data.	Ensure that the network cables are: • TIA/EIA-568A Category 5 twisted-pair Ethernet cables. • Properly installed.

Maintaining and upgrading the ENP-2611

Removing the ENP-2611

To remove the ENP-2611 from your Windows workstation:

1. Unplug the PC and all attached devices from power sources.
2. Remove:
   A. The PC cover, following the manufacturer's instructions.
   B. All cables from the board.
   C. SFP transceivers.
   D. The screw that secures the ENP-2611 to the rear panel of the PC.
3. Pull the ENP-2611 straight out of the slot.
4. Place the ENP-2611 on a flat, static-free surface.

3 Theory of Operation

The ENP-2611 is an Intel IXP2400 network processor-based board with three Gigabit Ethernet ports for fast-path data plane traffic.The ENP-2611 is designed in an industry-standard PCI form factor and features a PCI-to-PCI bridge that allows operation of the PCI bus at 64-bit width and speeds of up to 66MHz.

When reading this file online, you can immediately view information about any ENP-2611 topic by placing the mouse cursor over the topic name and clicking:

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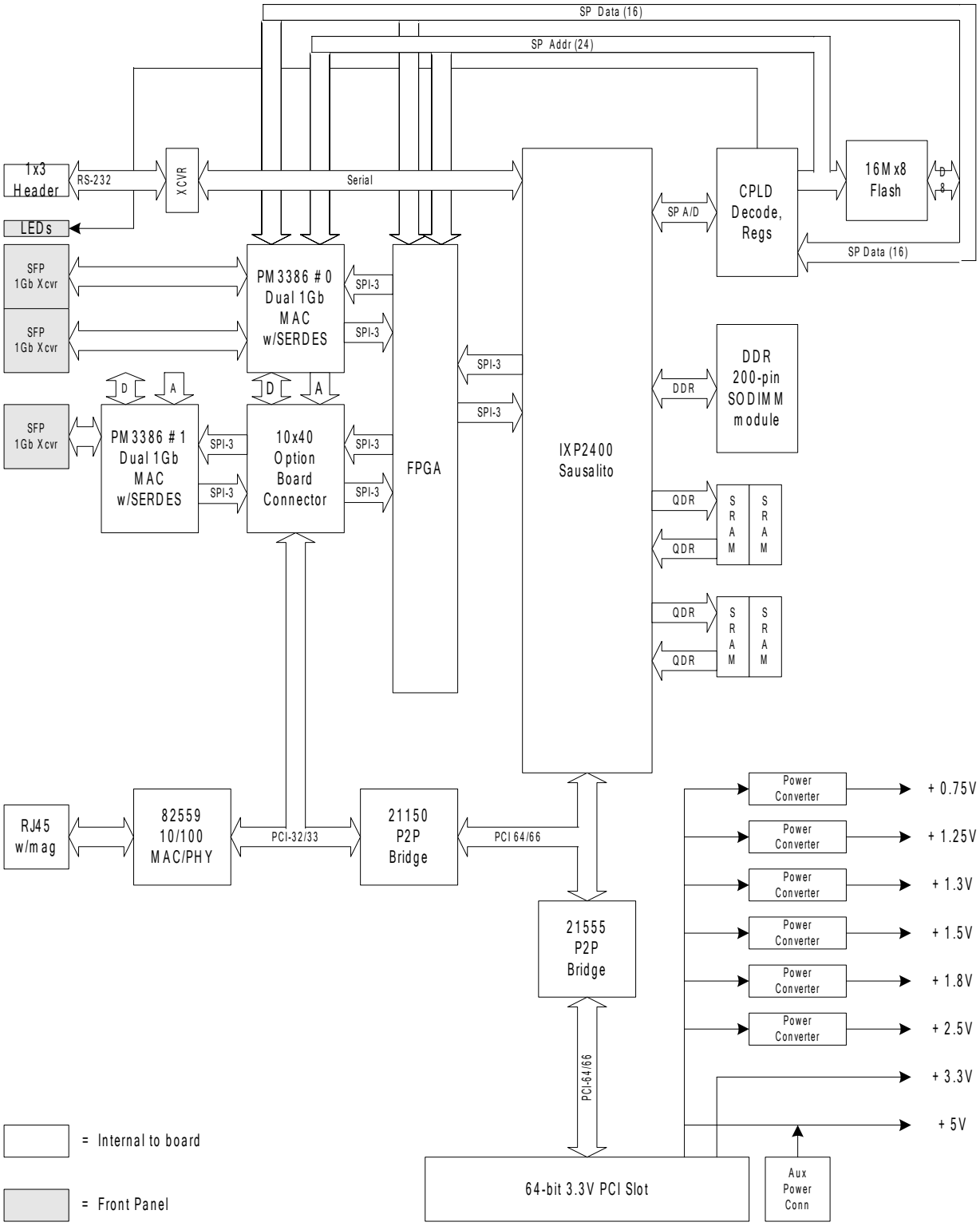
Block Diagram

Figure 3-1. Block Diagram



IXP2400 Network Processor

The ENP-2611 is based on an Intel IXP2400 network processor running at 600 MHz. Higher frequency processors are expected in the future, and the board accepts any compatible version.

The major blocks of the IXP2400 Processor are listed below.

XScale Core Processor

The XScale core consists of one 32-bit RISC processor compatible with the ARM Version 5 architecture. It implements the integer instruction set of ARM V5, but does not provide hardware support of the floating point instructions. The XScale initializes and manages the chip, and performs higher-layer network processing tasks.

Microengines (MEs)

The Microengines do most of the programmable packet processing in the IXP2400. Eight 32-bit programmable Microengines have access to all shared resources (SRAM, DRAM, MSF, etc.) as well as private connections between adjacent Microengines ("next neighbors").

The Microengine architecture provides support for software-controlled multi-threaded operation. Given the disparity in processor cycle times vs. external memory access times, a single thread of execution often blocks waiting for external memory operations to complete. Having multiple threads available allows for threads to interleave operation, which means there is often at least one thread ready to run while others are blocked.

- 16KB Scratchpad Memory for general-purpose use.
- MSF (Media and Switch Fabric Interface). This is the interface for network framers and/or switch fabric. It contains transmit and receive buffers.
- Hash Unit. The X-Scale and Microengines can use this to offload hash calculations.
- 64-bit Rev 2.2 PCI Controller.
- CAP (Chip-wide control and status registers). These provide interprocessor communication features.
- XPI (X-Scale Peripheral Interface). This consists of the Interrupt Controller, Timers, UART, GPIO (General-purpose I/O), and Slow Port Interface to off-chip peripherals.
- Performance Monitor. These counters can be programmed to count internal hardware events to analyze and tune performance.

DDR SDRAM

The DRAM memory controller within the IXP2400 supports a single 64-bit (72 bits with ECC) channel of Double-Data-Rate (DDR) SDRAM. A maximum memory address space of 2GB is allocated to DRAM. ECC (Error-Correcting Code) is supported by the IXP2400, but can be disabled. Enabling ECC requires that x72 memory be installed. Only DDR memory with concurrent auto-precharge is supported by IXP2400.

The ENP-2611 provides a standard laptop-style 200-pin right-angle SODIMM socket to house a single DDR SDRAM SODIMM memory module. This allows the board to occupy a single PCI slot. This interface conforms to the *JEDEC PC2100 DDR SDRAM Unbuffered SO-DIMM Reference Design Specification Revision 1.0*.

The socket is keyed to only allow installation of +2.5V modules.

DDR memory modules have a serial EEPROM which contains information about the DRAM size, density, speed, etc. The serial EEPROM must be read by software running on the IXP2400 XScale processor to configure the memory controller properly. The EEPROM is connected to GPIO pins on the IXP2400. For details, see *IXP2400 GPIO Pin Assignments* on page 49. The serial EEPROM resides at Address 1010000b of the serial bus.

QDR SRAM

The IXP2400 has two independent SRAM controllers, each supporting pipelined QDR synchronous SRAM and/or a coprocessor that adheres to QDR interface signaling. The SRAM is accessible by the Microengines, the XScale core, and the PCI unit.

The memory is logically four bytes wide; physically the data pins are two bytes wide and are double-clocked. Byte parity is supported, resulting in the use of x18 SRAM devices. Each QDR SRAM channel on the IXP2400 allows a maximum memory address space of 64MB, and a maximum of 4 loads. All the SRAMs on a given channel must be the same size and vendor.

ENP-2611 QDR Implementation

The ENP-2611 uses one or two 2Mx18 QDR II (1.8V) SRAMs on each of the two QDR channels, for a total of 8MB (one per channel) or 16MB (two per channel).

Scratchpad Memory

The IXP2400 contains a 16KB Scratchpad Memory, organized as 4K 32-bit words, accessible by the Microengines and XScale core.

Scratchpad Memory provides the following operations:

- Normal reads and writes. From one to 16 32-bit words can be read/written with a single Microengine instruction. Note that Scratchpad Memory is not byte-writable.
- Atomic read-modify-write operations.
- 16 hardware-assisted rings for interprocess communication.

Scratchpad Memory is provided as a third memory resource, in addition to SRAM and DRAM, that is shared by the Microengines and XScale core. The Microengines and XScale core can distribute memory accesses between these three types of memory resources to increase the number of memory accesses occurring in parallel.

Media and Switch Fabric (MSF) Interface

MSF Overview

The MSF (Media and Switch Fabric) Interface is used to connect the IXP2400 to a PHY (physical layer) device and/or to a switch fabric. The MSF consists of separate receive and trasmit interfaces. Each of the receive and transmit interfaces can be separately configured for either UTOPIA (Level 1, 2, and 3), POS-PHY (Level 2 and 3) or CSIX protocols.

The receive and transmit ports are unidirectional and completely independent of each other. Each port has 32 data signals, two clocks, a set of control signals, and a set of parity signals, all of which use 3.3V LVTTL signaling. The MSF bus operates from 25 to 125 MHz, and all signals are sampled on the rising edge of the clock.

ENP-2611 MSF Implementation

The ENP-2611 operates both the receive and transmit interfaces in 32-bit POS-PHY mode, connecting to a single FPGA SPI-3 Bridge device. The FPGA is a multiplexing device and bridges between two devices with POS-PHY (SPI-3) interfaces. It routes data between the IXP2400 and one of the POS-PHY ports. POS-PHY Level 3 Multi-PHY (MPHY) mode with in-band addressing is used to address the different ports. The interface to the FPGA operates at 104 MHz.

For more information, see *FPGA SPI-3 Bridge* on page 24.

Hash Unit

The IXP2400 contains a Hash Unit that can take 48-bit, 64-bit or 128-bit data and produces a 48-bit, a 64-bit or a 128-bit hash index, respectively. The Hash Unit is accessible by the Microengines and the XScale core, and is useful in doing table searches with large keys, for example L2 addresses.

PCI Controller

The PCI Controller on the IXP2400 provides a 64-bit, 66 MHz capable PCI Revision 2.2 interface. It is also compatible with 32-bit and/or 33 MHz PCI devices. The PCI Controller provides the following functions.

Target Access

There are three BARs (Base Address Registers) to allow other PCI bus masters to access the IXP2400 SRAM, DRAM, and CSRs, respectively. Other bus masters are the 82559 Ethernet Controller and the Host processor via the 21555 bridge.

The SRAM BAR can be programmed to sizes of 16 MB, 32 MB, 64 MB, 128 MB, or no access.

The DRAM BAR can be programmed to sizes of 128 MB, 256 MB, 512 MB, 1 GB, or no access.

The CSR BAR is fixed at 8 KB.

PCI Boot Mode is supported in hardware, in which the Host downloads the XScale core boot image through the 21555 bridge into IXP2400 DRAM, while holding the XScale core in reset. Once the boot image is loaded, reset is negated, allowing the XScale to boot from the image.

Master Access

The XScale core and the Microengines can directly access the local PCI bus, and can also access the Host's PCI bus if Upstream BARs in the 21555 bridge are properly programmed. The XScale core can do loads and stores to specific address ranges to generate all PCI command types.

DMA Channels

There are three DMA channels, each of which can move blocks of data from DRAM to PCI or PCI to DRAM. The DMA channels read parameters from a list of descriptors in SRAM, perform the data movement to or from DRAM, and stop when the list is exhausted. Up to three DMA channels can run at a time, with the active channels interleaving bursts to or from the PCI bus. There is no restriction on byte alignment of the source address or the destination address.

Interrupts are generated at the end of DMA operations to the XScale core. Microengines do not provide an interrupt mechanism. The DMA channel instead uses an Event Signal to notify the particular Microengine on completion of DMA.

Mailbox and Message Registers

The IXP2400 provides Mailbox and Doorbell registers for communication between the XScale core and a device on the PCI bus.

Four 32-bit Mailbox registers are provided that can be read and written with byte resolution by both the XScale core and a PCI device. How the registers are used is application dependent, and the messages are not used internally by the PCI Unit. Mailbox registers are often used with Doorbell interrupts.

The Doorbell registers provide a method of generating an interrupt as well as encoding the purpose of an interrupt. The PCI Unit has a 32-bit Doorbell register that is used by a PCI device to generate an XScale core interrupt, and a separate 32-bit PCI Doorbell register that is used by the XScale core to generate a PCI interrupt.

PCI Arbiter

The PCI Unit contains a PCI bus arbiter that supports two external masters in addition to the PCI Unit's own initiator interface. If more than two external masters are used in the system, the arbiter can be disabled and an external (to IXP2400) arbiter used. In that case, IXP2400 provides its request signal to the external arbiter, and use that arbiter's grant signal.

Since there are only two other PCI devices on the Local64 PCI bus, the ENP-2611 uses the internal arbiter of the IXP2400. The Secondary PCI bus arbiter of the 21555 bridge is disabled.

CAP

The CAP (CSR Address Proxy) contains a number of chip-wide control and status registers. Some of these provide miscellaneous control and status, while others are used for inter-Microengine and Microengine-to-XScale core communication.

XScale Peripherals

The IXP2400 contains several peripherals that are accessible to the XScale core processor. They include the Interrupt Controller, Timers, GPIO pins, UART, Slow Port, and thermal diode interface.

Interrupt Controller

The Interrupt Controller provides the ability to enable or mask interrupts from a number of chip-wide resources, such as:

- Timers, which are normally used by the Real-Time Operating System
- Interrupts generated by Microengine software to request services from the XScale core
- External agents such as PCI devices
- Error conditions, such as DRAM ECC errors or MSF parity errors

Interrupt status is read from memory-mapped registers. The state of an interrupt signal can be read even if it is masked from interrupting. Enabling and masking of interrupts is dones as writes to memory-mapped registers.

Timers

The IXP2400 contains four programmable 32-bit timers. Each timer can be clocked by an internal clock, by a divided version of the clock, or by a signal on an external GPIO pin. Each timer can be programmed to generate a periodic interrupt after a programmed number of clocks.

Timer 4 can be used as a watchdog timer. In this usage, software must periodically reload the timer value. If if fails to do so and the timer expires, it resets the IXP2400.

GPIO

The IXP2400 contains eight General Purpose I/O (GPIO) pins. These can be programmed as either input or output and can be used for slow-speed I/O such as LEDs or input switches. They can also be used as interrupts to the XScale core, or to clock the programmable timers.

For details about pin usage on the ENP-2611, see *IXP2400 GPIO Pin Assignments* on page 49.

UART

The IXP2400 contains a standard RS-232 compatible UART, which can be used for serial communication with a debugger or maintenance console. Modem controls are not supported, just the TxD (Transmit) and RxD (Receive) signals.

The serial port can operate in either FIFO or non-FIFO mode. In FIFO mode, a 64-byte transmit FIFO holds data from the processor to be transmitted on the serial link and a 64-bit receive FIFO buffers data from the serial link until read by the processor.

The UART has a programmable baud rate generator, which is capable of dividing the internal clock input by divisors of 1 to $2^{16} - 1$, and produces a 16X clock to driver the internal transmit and receive logic. The UART can be operated in polled or interrupt-driven mode as selected by software.

The TxD and RxD signals from the UART are buffered with an RS-232 transceiver, and are available on a keyed 3-pin header at the top edge of the board. A custom null-modem serial cable is available which converts the 3-pin connector to a standard female DB-9 connector.

Slow Port

The IXP2400 Slow Port provides an external interface intended for access to a Flash Boot ROM and 8-bit, 16-bit and 32-bit asynchronous slave devices. It allows the XScale core or Microengines to do read/write data transfers to these slave devices. There are two ports (chip-selects) in the Slow Port unit. The first is dedicated to the Flash Boot ROM, and the second to the uP (slave) device.

The address bus and data bus are multiplexed to reduce pin count on the IXP2400. For each access to a slave device, up to 26 bits of address are shifted out in three clock cycles, requiring external latches to capture the address which is then presented to the device.

The access is asynchronous. Insertion of delay cycles for both data setup and hold time is programmable via internal Control registers. The transfer can also wait for a handshake acknowledge signal from the external device.

There are several peripherals connected to the Slow Port on the ENP-2611. A CPLD "glue" device is directly connected to the multiplexed Slow Port of the IXP2400, and it creates a non-multiplexed bus for the following peripherals:

- Flash Boot Device
- FPGA SPI-3 Bridge programming interface
- PM3386 and PM3387 Gigabit MAC programming interfaces
- Programming interface for the SPI-3 Option Board.

CPLD: A CPLD converts the IXP2400 Slow Port signals into a useable bus for the Flash and peripherals. It creates up to a 26-bit address bus from the multiplexed AD0-7, DIR/A1, and CP/A0 IXP2400 signals. For byte-wide target devices, it buffers and times the data between the IXP2400 and the target. For 16-bit target devices, it also performs byte-packing and unpacking. There are no 32-bit peripherals on the ENP-2611.

The 64MB address space of the IXP2400 Slow Port is divided into two halves. The lower 32MB is reserved for Flash and the FPGA, which operate in Mode 0 and use SP_CS_L0.

The upper 32MB is intended for peripherals such as framers, MACs, etc. with non-standard microprocessor interfaces. These may be 8-bit or16-bit devices with varying numbers of address inputs. This upper section operates in Mode 3 with a 16-bit

data interface, and is used to connect to the peripherals on the ENP-2611, which consist of the PM3386 and PM3387 Gigabit MACs and the SPI-3 Option Board.

Flash Boot Device: Only 8-bit Flash devices are supported by the IXP2400. The Flash devices supported includes:

- 16 MB StrataFlash

The ENP-2611 uses a single flash device operating in byte mode for a total of 16 MB of Flash.

The Slow Port operates in Mode 0 for the Flash device, using SP_CS_L0. In this mode, the full 26 bits are available. The Flash resides in the low 16MB of the Slow Port address space.

FPGA SPI-3 Bridge: An FPGA SPI-3 Bridge is connected between the MSF interface of the IXP2400 and the PM3386/7 Gigabit MAC devices. It routes data from one interface to another, and has several functions which must be programmed by software. Its programming interface is connected to the CPLD's non-multiplexed Slow Port.

The FPGA appears in the second 16MB of the Slow Port address space. The Slow Port operates in Mode 0 for the byte-wide FPGA device, sharing SP_CS_L0 with the Flash.

For details, see *Appendix D, SPI-3 Bridge register definitions*.

PM3386 and PM3387 Gigabit MACs: A PM3386 and a PM3387 Gigabit MAC device are physically connected to the FPGA SPI-3 Bridge and are in the data stream of the IXP2400 MSF interface. Each of them have a microprocessor interface for programming the device that consists of 11 address inputs and a 16-bit data bus.

The CPLD's non-multiplexed Slow Port is connected to the PM3386/7's. The Slow Port operates in Mode 3 for the PM3386/7 devices, using SP_CS_L1 as the chip-select. The IXP2400 Slow Port is programmed for 24 address bits and 16 data bits via the SP_ADC register in the CAP. PM3386 #0 resides in the third 16MB portion of the Slow Port address space. PM3387 #1 resides above PM3386 #0.

SPI-3 Option Board: The CPLD's non-multiplexed Slow Port is connected to the SPI-3 Option Board connector to allow programming of a microprocessor interface which may exist on a future board. It operates in Mode 3, using SP_CS_L1 as the chip-select. The IXP2400 Slow Port is programmed for 24 address bits and 16 data bits via the SP_ADC register in the CAP.

Thermal Diode: The IXP2400 contains a thermal diode to allow remote monitoring of the die temperature. This feature is currently undocumented by Intel. The THERMDA and THERMDC pins are connected to an I^2C thermal diode temperature sensor. The I^2C serial bus pins and the thermal interrupt output of the sensor are connected to GPIO pins on the IXP2400 as described in the IXP2400 GPIO Pin Assignments section. A software driver is needed to generate the proper timing for the SCL and SDA signals in order to read the sensor. The temperature sensor resides at Address 1001100b of the serial bus.

Media Interfaces

FPGA SPI-3 Bridge

An FPGA SPI-3 Bridge is connected between the MSF interface of the IXP2400, which is operated in POS-PHY Level 3 (aka SPI-3, aka PL3) mode, and the PM3386 and PM3387 Gigabit MAC devices. Its function is to route data from one interface to another. For details about the FPGA, see *Appendix D, SPI-3 Bridge register definitions*.

POS-PHY Level 3 was developed by the SATURN Development Group to cover all application bit rates up to and including 3.2 Gbit/s. This interface provides standards support for interoperation between the PM3386, a multiple PHY layer device, connecting to one Link Layer device. The POS-PHY Level 3 interface is defined as either an 8-bit or 32-bit wide interface with a clock rate from 60 to 104 MHz.

The MSF-to-FPGA interface is implemented as a 32-bit bus operating at 104 MHz or higher. The FPGA-to-PM3386/7 interfaces are implemented as 32-bit busses operating at 104 MHz.

PM3386 and PM3387 Gigabit Ethernet Controllers

The PMC-Sierra PM3386 is a monolithic integrated circuit that implements a two port full duplex 1000 Mbit/s Gigabit Ethernet MAC data transport device. The PM3386 provides line interface connectivity provided by an on-chip SERDES and GMII functions and data transport to the upstream device via the industry standard POS-PHY Level 3 interface. The PM3387 is a single-port version of the PM3386, with the same functionality.

Serializer-Deserializer (SERDES)

The PM3386/7 has two internal serializer-deserializer transceivers. The SERDES are IEEE 802.3-1998 Gigabit Ethernet compatible supporting gigabit data transfer flows. The SERDES is based on the X3T11 10 Bit specification. The PM3386/7 receives and transmits Gigabit Ethernet streams using a bit serial interface for direct connection to optical transceiver devices. The SERDES performs data recovery and serial to parallel conversion for connection to the Enhanced Gigabit Media Access Control block.

EGMAC (Enhanced Gigabit Media Access Control)

The EGMAC (Enhanced Gigabit Media Access Control) block provides an integrated IEEE 802.3-1998 Gigabit Ethernet MAC (Media Access Control) supporting 1000Base capability. The EGMAC has line side interfaces for connection to internal (SERDES) and external Gigabit PHYs via GMII on each Gigabit Ethernet port. The EGMAC incorporates all of the Gigabit Ethernet MAC functions including Auto-Negotiation, statistics, and the MAC Control Sub-layer that adheres to IEEE 802.3-1998, and provides support for PAUSE control frames. The EGMAC provides basic frame integrity checks to validate incoming frames. It also provides simple line rate ingress address filtering support via 8 exact-match MAC address and VID unicast filters, one 64-bin hash-based multicast filter, and the ability to filter or accept matched frames on a per instance programmable fashion. All inquires for filtering are done at line rate with no system latency introduced for look up cycles.

Management Statistics (MSTAT)

The PM3386/7 also incorporates a set of per port RMON, SNMP, and Etherlike Management Information Base counters. Statistical counters are used for management counts providing a minimum rollover time of greater than 58 minutes. All counts are managed via the MSTAT (Management Statistics) block.

POS-PHY Level 3 Interface

The PM3386/7 can connect to a single upper layer device through a POS-PHY Level 3 (SPI-3) inerface. On the ENP-2611, each PM3386/7 device is connected to one of the ports of the FPGA SPI-3 Bridge. The POS-PHY interface contains 64KB receive and 16KB transmit FIFOs per channel. These FIFOs contain programmable thresholds specifying full and empty conditions.

Receive Direction

In the receive direction, the PM3386/7 can be configured to use the internal SERDES or the GMII interface on a per channel basis. For SERDES operation, a Gigabit Ethernet bit stream is received from an external optical transceiver. The data is recovered and converted from serial to parallel data for connection to the EGMAC block. The EGMAC terminates the 8B/10B line codes and performs frame integrity checks (frame length, FCS etc). For GMII operation, the physical packet is sourced from an external copper physical layer device to the PM3386/7 via the GMII interface (8 bits clocked at 125 MHz). The EGMAC accepts the 8 bit data and performs frame integrity checks once the complete frame is received. The EGMAC can optionally filter erred frames.

Statistics are updated and the frame is sent to the POS-PHY Level 3 interface. The FIFOs in the POS-PHY interface accommodate system latencies and allows for loss-less flow control of frames up to 9.6k bytes (Jumbo frames) in size. The received frames are then read through the POS-PHY Level 3 system side interface.

Transmit Direction

In the transmit direction, packets to be transmitted are written into the POS-PHY TX FIFO through the POS-PHY Level 3 interface from the upper layer device. The channel is selected by the upper layer device and is indicated in-band on the POS-PHY interface. The EGMAC builds a properly formatted Ethernet physical packet (padding to minimum size and inserting the preamble, start of frame delimiter (SFD) and the IPG (Inter-Packet Gap)). Statistics are updated and the physical packet is sent to the SERDES or the GMII interface.

For SERDES operation, the EGMAC encodes the physical packet using 8B/10B encoding and passes the physical packet to the SERDES block. The SERDES performs parallel to serial conversion using an internally synthesized 1250 MHz clock. The bit stream is sent to an external optical transceiver for transmission over fiber cable. For GMII operation, the EGMAC sends the physical packet byte by byte across the GMII interface (8 bits clocked at 125 MHz) to an external copper Gigabit Ethernet physical layer device. The copper Gigabit Ethernet physical layer device then transmits the physical packet over copper cable.

Flow Control

Flow control is handled in the EGMAC block. When a PAUSE control frame is received, the PM3386/7 optionally terminates transmission (after the current frame is sent) and asserts the appropriate channel sideband flow control output to indicate the paused condition. The received PAUSE control frame can be optionally filtered or passed to the link layer device via the POS-PHY Level 3 interface.

PAUSE control frames are transmitted either under link layer control using channel side band flow control inputs, under link layer control transparent to the PM3386/7, host based PAUSE frame control or under internal control based on receive FIFO levels. All four methods can provide for loss-less flow control.

Microprocessor Interface

The PM3386/7s are configured, controlled and monitored via a generic 16-bit microprocessor bus interface, described earlier in PM3386 and PM3387 Gigabit MACs.

Each PM3386/7 can be programmed to generate an interrupt based on several events. The interrupt pin on each PM3386/7 is connected to a GPIO pin on the IXP2400, which must be configured as an interrupt source.

For the location of the PM3386/7s within the memory map, see *IXP2400 Memory Map* on page 43. For details of the interrupt pins, see *IXP2400 GPIO Pin Assignments* on page 49.

Gigabit Ethernet Channels

The ENP-2611 provides three 1000BaseSX optical fiber Ethernet channels or three 1000Base-T Copper Ethernet channels, available on the front bracket of the board. The PM3386 Dual Gigabit Ethernet controller (PM3386 #0) described above is dedicated to the Port 0 and Port 1 channels using the SERDES interfaces. The PM3387 Gigabit Ethernet controller (PM3387 #1) is dedicated to the Port 2 channel. The GMII interfaces on both PM3386/7s are unused. The data signals to/from the SERDES connect through a standard 20-pin right-angle MSA-compliant connector to a transceiver.

The optical tranceivers are implemented with SFP (Small Form-factor Pluggable) LC transceiver modules that plug into MSA-compliant connectors and shielded cages. 50 µm or 62.5 µm multimode fiber cables terminated with LC style connectors are required for connection to the modules.

An automatic shutdown circuit is built into the transceiver module that disables the laser when it detects laser faults, which ensures compliance to Eye Safety requirements.

The copper tranceivers are implemented with SFP (Small Form-factor Pluggable) RJ-45 transceiver modules that plug into MSA-compliant connectors and shielded cages. CAT-5 cables terminated with RJ-45 style connectors are required for connection to the modules.

Type information concerning which kind of SFP module is plugged into the port is available on the modules' MOD-DEF interface. The information is stored in an I^2C EEPROM inside each transceiver module. The MOD-DEF interface on each transceiver is accessed through separate 2-wire serial interfaces located in the Transceiver registers

in the CPLD. The serial information definition for the EEPROM in the tranceivers is defined in the *Small Form Factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA)*. For more information about this document, see *Where to get more information* on page iv.

The transmitter within each transceiver can be disabled under software control via the TX_DISABLE bit. There is a TX_FAULT status signal associated with each transceiver. This signal is asserted if the transceiver is not installed, or a fault is detected by the transmitter safety circuitry. There is also a LOS (Loss Of Signal) status signal for each transceiver. This signal is asserted if the link is outside the required values for proper operation.

All three of these signals can be accessed through the Transceiver registers in the CPLD. In addition, their state displays on LEDs visible through the front bracket of the non-MP version.

Neither the transceiver nor the PM3386/7 Ethernet Controller provide signals which indicate Ethernet activity or errors. The PM3386/7 does have a number of internal registers which provide this information. A fourth LED on the non-MP version for each channel connected to the Transceiver registers in the CPLD, and can be used by software to display additional information about the channel.

Option Board Interface

A 400-pin BGA connector is provided on the ENP-2611 which allows expansion of the "PHY 1" channel of the SPI-3 FPGA to a future proprietary RadiSys-designed SPI-3 Option Board. The BGA connector is mounted on the rear side of the board, connecting to the Option Board in the slot behind the ENP-2611.

Two pins are used on the connector for each SPI-3 signal. This allows maximum flexibility in routing the PHY 1 channel from the FPGA to the Option Board and back to the ENP-2611. The standard ENP-2611 with no Option Board requires a small "shorting board" to be mated with the connector, so that the PHY 1 FPGA channel is connected through to PM3387 #1.

PCI Interfaces

The ENP-2611 includes three PCI busses.

- Host PCI 64-bit/66 MHz bus: Connects between the backplane and the Primary side of a 21555 non-transparent PCI/PCI bridge.
- Local64 64-bit/66 MHz bus: Connects between the Secondary side of the 21555, the IXP2400, and the Primary side of a PCI2050B transparent PCI/PCI bridge.
- Local32 32-bit/33 MHz bus: Connects between the Secondary side of the PCI2050B, the 82559 Ethernet controller, and the Option Board connector.

The ENP-2611 uses a Universal voltage, 64-bit/66 Mhz PCI bus edge connector that plugs into a host backplane connector. This interface is used for input power and to communicate with the host processor. The interface conforms to the PCI Local Bus

Specification Revision 2.3, with the exception that the board may draw more power than the maximum 25 Watt PCI specification.

Note

The ENP-2611 typically draws approximately 20–25 Watts from the backplane PCI connector, which is within specification of 25 Watts per slot. Maximum calculated power is approximately 40 Watts.

The 25 Watt specification is largely determined by system power allocation of the 200–250 Watt supply within a PC chassis. The pins of the backplane connector are specified to carry the current drawn by the ENP-2611.

The Host PCI interface has these characteristics:

- Standard full-length PCI form factor.
- JTAG scan is bypassed by connecting TDI to TDO.
- Input power is derived from both +3.3V and +5V.
- +12V is used to power the fansink for the IXP2400.
- VIO is used to power the I/O buffers of the bridge.
- The edge connector is keyed for both +5V and +3.3V (Universal) signaling.

Host (Backplane) PCI Bus

The Host PCI bus consists of the backplane into which the ENP-2611 is plugged. It can be either a 32-bit or 64-bit interface, and can be configured to run at either 33 or 66 MHz. A single device on the ENP-2611 connects to the Host PCI bus—the Primary side of a 21555 PCI/PCI bridge.

The ENP-2611 is 66 MHz-capable, and therefore does not drive the M66EN pin.

21555 PCI/PCI Bridge

The ENP-2611 uses the Intel 21555 PCI/PCI bridge as a bridge between the Host PCI bus on the backplane and the internal Local64 PCI bus. The device is a non-transparent PCI/PCI Bridge compliant with the PCI Local Bus specification Revision 2.2 on both its primary and secondary interfaces. The primary side of the bridge is connected to the Host PCI bus, and the secondary side is connected to the Local64 PCI bus.

The bridge provides the following features:

- Non-transparent operation, with independent address spaces on the two sides of the bridge.
- Independent bus clocks, allowing communication between the 33/66 MHz secondary bus and the 33/66 MHz host bus.
- Independent bus widths, allowing communication between the 64-bit secondary bus and the 32/64-bit host bus.

- +3.3VDC operation, with +5VDC-tolerant I/O, allowing use in either a +5V or 3.3V host slot.

Note

The terms "Downstream" and "Upstream" accesses and forwarding are used throughout the discussion of the 21555. Downstream means an access from the primary (backplane PCI bus) side of the bridge to the secondary (internal) side. Upstream means an access from the secondary side to the primary side.

The 21555 contains four BARs (Base Address Registers) for downstream transaction forwarding from the Host PCI bus to the PCI bus. One BAR is programmable as memory or I/O space and also contains CSRs specific to the 21555, the other three BARs forward memory transactions only. All of the BARs on the primary interface provide direct offset address translation.

The device also contains three BARs for upstream transaction forwarding from the internal PCI bus to the Host PCI bus. One BAR is programmable for memory or I/O transactions, and a second is used for forwarding memory transactions only. Both registers support direct offset address translation. A third BAR is used for forwarding memory transactions using LUT (Look Up Table) based address translation.

The bridge offers posted write data queues (256 Bytes) and delayed read data queues (256 Bytes) in both directions, as well as a delayed transaction queue supporting up to four pending transactions.

The 21555 contains a secondary PCI arbiter, but it is disabled on the ENP-2611. The IXP2400 serves as the Local64 PCI bus arbiter.

The 21555 core is powered from +3.3V, and has +5V tolerant I/O buffers. The internal (secondary) PCI interface uses the +3.3V PCI signaling environment. VIO on the primary PCI interface is connected to the backplane VIO supply to accommodate both +3.3V and +5V signaling environments.

The 21555 primary and secondary clocks run asynchronously. The primary clock is provided by the host, and may be either 33 MHz or 66 MHz. This clock is required in order for the Serial ROM configuration and the IXP2400's access to 21555 configuration registers to occur. The secondary clock is provided by a clock generator internal to the board, and connects to all devices on the Local64 PCI bus.

Doorbell Interrupts: A 16-bit software-controlled interrupt request register and an associated mask register are provided on the 21555 for both the primary and secondary interfaces. Each register is byte addressable so they can be used as two sets of 8-bit registers, if desired. They can be accessed from the primary or secondary interface of the 21555, in either memory or I/O space.

The primary interrupt pin (P_INTA#) is asserted low whenever one or more Primary Interrupt Request bits are set and their corresponding Primary IRQ Mask bits are 0. P_INTA# remains low as long as this condition exists. It is negated when either the Primary Interrupt Request bit is cleared or the Primary IRQ Mask bit is set. The secondary interrupt pin (S_INTA#) operates in an identical manner using the Secondary Interrupt and Mask registers. For details, see the *21555 Non-Transparent PCI/PCI Bridge User Manual*.

Scratchpad Registers: The eight 32-bit Scratchpad Registers in the 21555 can be accessed in either memory or I/O space from either the primary or secondary interfaces. These registers can be used to pass control and status information between primary and secondary bus devices, or treated as generic read/write registers. Reading or writing a Scratchpad Register does not cause an interrupt to be asserted. For details, see the *21555 Non-Transparent PCI/PCI Bridge User Manual*.

Configuration and Initialization: The 21555 contains two sets of configuration registers, one for each PCI interface, as well as device-specific configuration and status registers. Certain configuration registers can be preloaded at power-up using a serial ROM connected to the bridge. This allows the PCI interfaces in the device to be tailored to the specific implementation prior to the Host or IXP2400 processor access to PCI configuration space. The serial ROM unloads automatically at power-up and signals a Target Retry on both PCI interfaces until the serial ROM preload sequence completes. In this configuration the local processor can overwrite the configuration values, loaded by the serial ROM at power-up by using secondary PCI configuration space accesses. The next table defines the serial ROM default values used to pre-configure the bridge at power-up.

Table 3-1. 21555 Serial Preload Values

Byte Offset	Description	Preload Value	Comment
00h	Bit [7] 1 to enable serial preload Bits 6:0] 0000000b (Reserved)	80h	Enabled
01h	00000000b (Reserved)	00h	
02h	00000000b (Reserved)	00h	
03h	00000000b (Reserved)	00h	
04h	Primary Programming Interface	00h	As defined by PCI
05h	Primary Sub-Class Code	80h	As defined by PCI
06h	Primary Base Class Code	06h	As defined by PCI
07h	Subsystem Vendor ID [7:0]	31h	RadiSys Subsystem Vendor ID
08h	Subsystem Vendor ID [15:8]	13h	RadiSys Subsystem Vendor ID
09h	Subsystem ID [7:0]	30h	ENP-2611
0Ah	Subsystem ID [15:8]	00h	ENP-2611
0Bh	Primary Minimum Grant	04h	Minimum burst time required for the 21555 to master the local PCI bus in ¼ uS increments (1uS @ 33MHz)
0Ch	Primary Maximum Latency	28h	Specifies how often the 21555 needs to master the host PCI bus in ¼ uS increments (10uS @ 33MHz)
0Dh	Secondary Programming Interface	00h	As defined by PCI
0Eh	Secondary Sub-Class Code	80h	As defined by PCI
0Fh	Secondary Base Class Code	06h	As defined by PCI
10h	Secondary Minimum Grant	04h	Minimum time required for the 21555 to master the local PCI bus in ¼ uS increments (1uS @ 33MHz)

Table 3-1. 21555 Serial Preload Values

Byte Offset	Description	Preload Value	Comment
11h	Secondary Maximum Latency	30h	Specifies how often the 21555 needs to master the local PCI bus in ¼ uS increments (10uS @ 33MHz)
12h	Downstream Memory 0 Setup [7:0] Bits [7:4, 0] are not loaded and should be 0.	00h	4 KB Memory space, no prefetch
13h	Downstream Memory 0 Setup [15:8] Bits [11:8] are not loaded and should be 0.	00h	4 KB Memory space, no prefetch
14h	Downstream Memory 0 Setup [23:16]	00h	32KB Memory space, no prefetch
15h	Downstream Memory 0 Setup [31:24]	00h	4 KB Memory space, no prefetch
16h	Downstream I/O or Memory 1 Setup [7:0] Bits [5:4] are not loaded and should be 0.	00h	Disabled
17h	Downstream I/O or Memory 1 Setup [15:8]	00h	Disabled
18h	Downstream I/O or Memory 1 Setup [23:16]	00h	Disabled
19h	Downstream I/O or Memory 1 Setup [31:24]	00h	Disabled
1Ah	Downstream Memory 2 Setup [7:0] Bits [7:4, 0] are not loaded and should be 0.	00h	Disabled
1Bh	Downstream Memory 2 Setup [15:8] Bits [11:8] are not loaded and should be 0.	00h	Disabled
1Ch	Downstream Memory 2 Setup [23:16]	00h	Disabled
1Dh	Downstream Memory 2 Setup [31:24]	00h	Disabled
1Eh	Downstream Memory 3 Setup [7:0] Bits [7:4, 0] are not loaded and should be 0.	00h	Disabled
1Fh	Downstream Memory 3 Setup [15:8] Bits [11:8] are not loaded and should be 0.	00h	Disabled
20h	Downstream Memory 3 Setup [23:16]	00h	Disabled
21h	Downstream Memory 3 Setup [31:24]	00h	Disabled
22h	Downstream Memory 3 Setup Upper 32 Bits [7:0]	00h	Disabled
23h	Downstream Memory 3 Setup Upper 32 Bits [15:8]	00h	Disabled
24h	Downstream Memory 3 Setup Upper 32 Bits [23:16]	00h	Disabled
25h	Downstream Memory 3 Setup Upper 32 Bits [31:24]	00h	Disabled
26h	Bits [7:4]: Primary Expansion ROM Setup [15:11] Bits [3:1]: Not loaded. Should be 0. Bit [0]: Primary Expansion ROM Setup [24] (enable)	00h	Disabled
27h	Primary Expansion ROM Setup [23:16]	00h	Disabled
28h	Upstream I/O or Memory 0 Setup [7:0] Bits [5:4] are not loaded and should be 0.	00h	Disabled
29h	Upstream I/O or Memory 0 Setup [15:8]	00h	Disabled
2Ah	Upstream I/O or Memory 0 Setup [23:16]	00h	Disabled
2Bh	Upstream I/O or Memory 0 Setup [31:24]	00h	Disabled

Table 3-1. 21555 Serial Preload Values

Byte Offset	Description	Preload Value	Comment
2Ch	Upstream Memory 1 Setup [7:0] Bits [7:4, 0] are not loaded and should be 0.	00h	Disabled
2Dh	Upstream Memory 1 Setup [15:8] Bits [11:8] are not loaded and should be 0.	00h	Disabled
2Eh	Upstream Memory 1 Setup [23:16]	00h	Disabled
2Fh	Upstream Memory 1 Setup [31:24]	00h	Disabled
30h	Chip Control 0 [7:0]	00h	
31h	Chip Control 0 [15:8] Bits [13:12] are not loaded and should be 0.	0Ch	Primary Lockout bit set, must be cleared by the local processor to enable Host processor configuration. Secondary clock output disabled
32h	Chip Control 1 [7:0]	00h	No subtractive decode
33h	Chip Control 1 [15:8]	00h	Upstream Memory 2 BAR Disabled, I2O unit disabled
34h	Arbiter Control [7:0]	00h	Arbiter not used
35h	Arbiter Control [15:7] Bits [15:10] are not loaded and should be 0.	02h	Arbiter not used
36h	Primary ~SERR Disable Bit [7] is not loaded and should be 0.	00h	All conditions unmasked
37h	Secondary ~SERR Disable Bit [7] is not loaded and should be 0.	00h	All conditions unmasked
38h	Power Management Data 0	00h	Not Used - Disabled
39h	Power Management Data 1	00h	
3Ah	Power Management Data 2	00h	
3Bh	Power Management Data 3	00h	
3Ch	Power Management Data 4	00h	
3Dh	Power Management Data 5	00h	
3Eh	Power Management Data 6	00h	
3Fh	Power Management Data 7	00h	
40h	Compact PCI Hot Swap ECP ID	00h	Assigned by the PCI SIG
41h	Bits [7:6] Power Management Capabilities Register [1:0] Bits [5:4] Power Management Control and Status[14:13] Bit [3] Power Management Data Register Enable Bit [2] BiST Supported Bits [1:0] 00b (Reserved)	00h	No BIST support, Power Management disabled
42h	Bits [7:2] Power Management Capabilities Register [14:9] Bit [1] Power Management Capabilities Register [5] Bit [0] Power Management Capabilities Register [2]	00h	

The next table shows the address translation window mapping through the bridge. This map may be altered for a specific platform by firmware overwriting the defaults established by the serial ROM preload.

Table 3-2. Address Translation Window Configuration

Base Address Register	Specific Usage	Translation Type
Primary Memory-mapped CSRs & Downstream Memory 0	21555 Registers, no forwarding range	Direct offset translation (above 4 KB)
Primary I/O-mapped CSRs	21555 Registers	None
Downstream Memory or I/O 1	Not programmed, configurable by application code	Direct offset translation
Downstream Memory 2	Not programmed, configurable by application code	Direct offset translation
Downstream Memory 3	Not programmed, configurable by application code	Direct offset translation
Secondary Memory-mapped CSRs	21555 Registers	None
Secondary I/O-mapped CSRs	21555 Registers	None
Upstream Memory or I/O 0	Not programmed, configurable by application code	Direct offset translation
Upstream Memory 1	Not programmed, configurable by application code	Direct offset translation
Upstream Memory 2	Not programmed, configurable by application code	Look up table

Local64 PCI Bus

The Local64 PCI bus consists of three devices on the ENP-2611. They are the secondary side of the 21555 PCI-to-PCI bridge, the IXP2400 Network Processor, and the PCI2050B transparent PCI/PCI bridge. This bus is configured for 64-bit 66 MHz operation and uses +3.3V signaling.

Clocking

The 21555 primary and secondary clocks run asynchronously. The Local64 PCI bus clocks are provided by a 66 MHz clock generator internal to the board, and connect to devices on that bus.

Arbitration

The pr_ad7 input pin on the 21555 is strapped low and the GPIO2 input pin on the IXP2400 is strapped high during reset, forcing the IXP2400 to serve as the arbiter for the local PCI bus. The 21555, the IXP2400, and the PCI2050B can all request to be the bus master of the Local64 PCI bus.

Interrupts

The IXP2400 serves as the host for interrupts on the Local64 PCI bus. Interrupts can be generated to the IXP2400 by the secondary side of the 21555, the 82559, a PCI device on the Option Board, or by the PCI Unit on the IXP2400 itself. The PILM field of

the IXP2400's XSCALE_INT_ENABLE register reflects the status of the two PCI interrupt pins.

The Host PCI processor can interrupt the IXP2400 by setting bits in the 21555's Secondary Set/Clear and Set Mask/Clear Mask Registers. This causes the 21555 to assert it s_inta_l pin, interrupting the IXP2400. Another way is to open a Downstream BAR on the 21555 to point to the PCI CSR Registers of the IXP2400, and set a bit in the XSCALE_DOORBELL register.

Similarly, the IXP2400 can interrupt the backplane host processor by setting bits in the 21555's Primary Set/Clear and Set Mask/Clear Mask Registers. This causes the 21555 to assert its p_inta_l pin, interrupting the Host PCI bus.

IXP2400 Network Processor

For details, see the PCI Controller section of the IXP2400.

Local32 PCI Bus

The Local32 PCI bus consists of three devices on the ENP-2611. They are the secondary side of the PCI2050B PCI-to-PCI bridge, the 82559 Ethernet controller, and possibly a PCI device on the SPI-3 Option Board. This reduced-width 33 MHz bus allows the use of the 82559, and simplifies connection of the Option Board. This bus is configured for 32-bit 33 MHz operation and uses +3.3V signaling.

PCI2050B PCI/PCI Bridge

The ENP-2611 uses the TI PCI2050B PCI/PCI bridge as a bridge between the Local64 PCI bus and thel Local32 PCI bus. The device is a transparent PCI/PCI Bridge compliant with the PCI Local Bus specification Revision 2.2 on both its primary and secondary interfaces. The primary side of the bridge is connected to the Local64 PCI bus, and the secondary side is connected to the Local32 PCI bus.

Clocking

The PCI2050B bridge is used to generate the clocks for the Local32 bus. It is configured as the clock generator on power-up. The Local32 PCI bus operates at 33 MHz.

Arbitration

The PCI2050B bridge serves as the arbiter for the Local32 PCI bus. The 82559 and possibly a PCI device on the Option Board can request to be the bus master of the Local32 PCI bus. The PCI2050B arbiter supports a two-level rotating priority algorithm, where two groups of masters can be assigned: a high-priority group and a low-priority group. Any of the masters can be assigned to any group via the PCI2050B's ARBITER_CONTROL register.

Interrupts

The IXP2400 serves as the host for interrupts on the Local32 PCI bus as well as the Local64 bus. Local32 device interrupts do not pass through the PCI2050B; they are connected directly to the IXP2400.

82559 10BaseT/100Base-TX Ethernet Controller

The ENP-2611 contains an Intel 82559 Fast Ethernet controller which incorporates internal MAC (Media Access Controller) and PHY (PHYsical interface) interfaces, providing support for 10Base-T or 100Base-TX connections. The Ethernet controller resides on the Local32 PCI bus, and has a standard PCI 2.1 compliant configuration space allowing system identification and configuration. For interrupt and ~REQ/~GNT assignment information, see the Programming section of this document.

The 82559's PHY enables direct connection to the network media using a 25 MHz, ±50 ppm crystal to derive its internal transmit digital clocks. The PHY connects to an RJ45 connector containing integrated magnetics. The connector is accessible on the top edge of the board. In 100Base-TX mode, the analog subsection of the PHY performs two functions:

- Takes received analog data from the RD pair and converts it into a digital 125 Mbps stream, recovering both clock and data.
- Converts a digital 125 Mbps stream into the proper format and drive it through the TD pair into the physical medium.

The 82559 provides Link and Activity LED indicators capable of sinking 10 mA. The 82559 directly drives the Link and Activity LEDs that are integral to the RJ45 connector.

Option Board PCI Interface

The Local32 PCI bus connects to the SPI-3 Option Board connector, allowing a PCI device to reside on that board. The Local32 PCI interface to the Option Board is intended for programming and maintenance. It is not expected that the main traffic payload utilizes this bus.

A single ~REQ/~GNT pair is routed from the PCI2050B Secondary side to the connector, providing bus master accesses for the device on the Option Board. A single interrupt signal is shared with the 82559, and connects to a PCI interrupt on the IXP2400.

Clocking

IXP2400 System Clock Generation

The system reference clock for the IXP2400 is generated by a 100 MHz oscillator.

IXP2400 MSF/FPGA Interface Clock Generation

The MSF interface between the IXP2400 and the FPGA SPI-3 Bridge is operated in POS-PHY mode. According to the POS-PHY Level 3 specification, the clock frequency can range from 60 MHz to 104 MHz. However, the IXP2400 is specified to run up to 125 MHz .

The MSF transmit and receive clocks are generated by a 104 MHz oscillator.

The output of the clock generator is applied to a low-skew clock buffer, which drives copies of the clock to the TFCLK and RFCLK pins on both the IXP2400 and the FPGA.

FPGA/PM338x Interface Clock Generation

The POS-PHY Level 3 (SPI-3) interface between the FPGA SPI-3 Bridge and the PM3386/7 Gigabit Ethernet controllers are operated in POS-PHY mode. According to the POS-PHY Level 3 specification, the clock frequency can range from 60 MHz to 104 MHz.

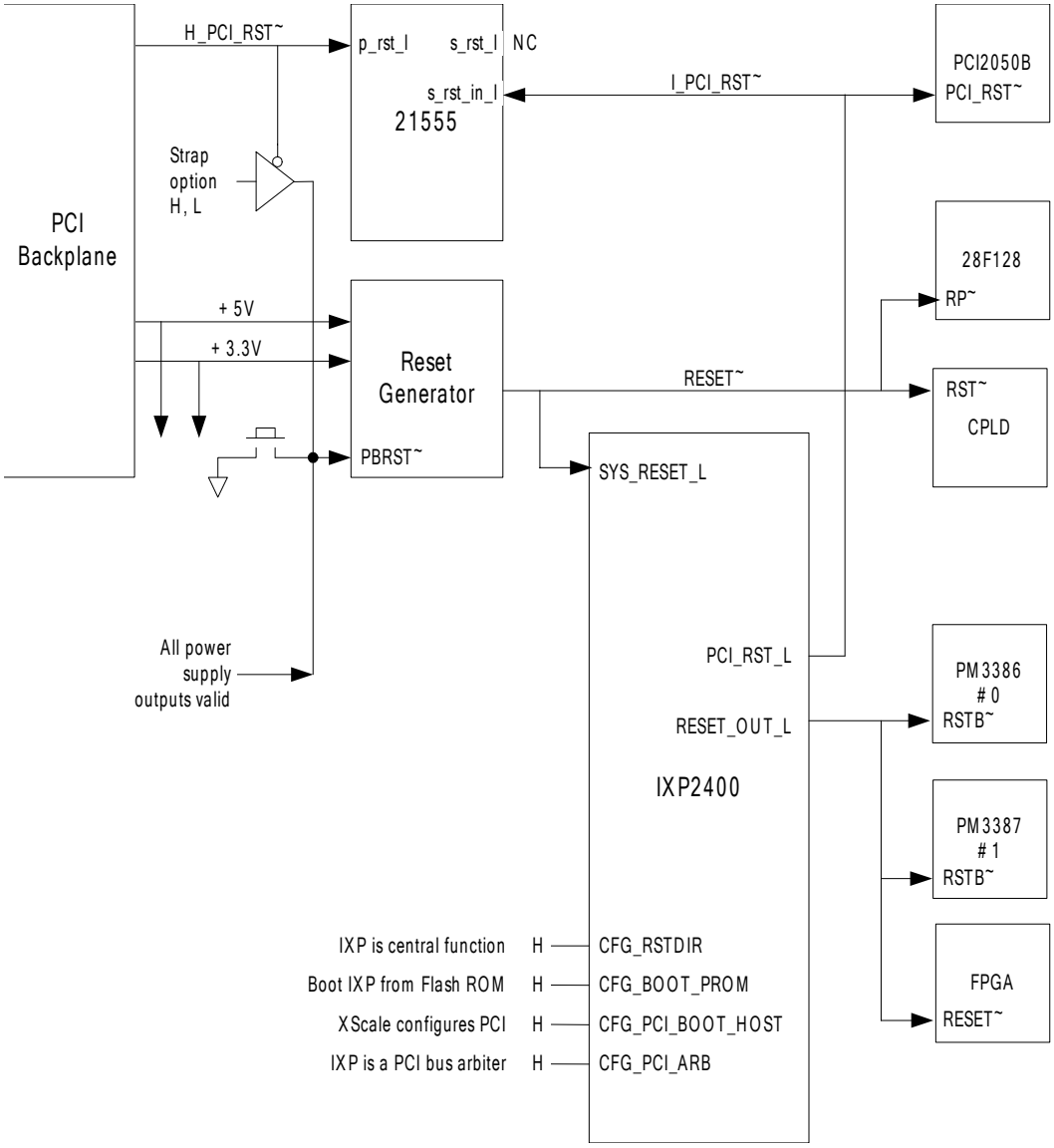
The FPGA and PM3386/7 transmit and receive clocks are generated by a 104 MHz oscillator.

The output of the clock generator is applied to a low-skew clock buffer, which drives copies of the clock to the TFCLK and RFCLK pins on both the FPGA and the PM3386/7 devices.

Reset and Initialization

The next figure shows a block diagram of the ENP-2611's reset circuitry.

Figure 3-2. Reset Generation



Upon power-up, the reset generator checks the backplane +5V and +3.3V power supplies. When the backplane voltages are within tolerance, the various onboard power supplies are sequentially enabled. During this time, reset is asserted to the IXP2400, and all other peripherals.

Each of the onboard power supplies has a comparator circuit which determines if its output voltage is above a prescribed threshold. All of their comparator outputs, the internal pushbutton reset and optionally the backplane PCI reset are logically OR'ed together and applied to the reset input of the micro-monitor chip.

Once all of the internal supplies are within tolerance, reset is negated to the IXP2400, and it goes through its power-up reset sequence. Since the IXP2400 is configured to be the PCI central function via the CFG_RSTDIR pin, it controls the negation of reset to the rest of the peripherals.

If any of the following conditions occur, the SYS_RESET_L input is asserted to the IXP2400 resulting in all downstream peripherals being reset via its PCI_RST_L output.

- A failure occurs on any power supply.
- The internal pushbutton reset is pressed.
- Optionally, the backplane PCI reset is asserted. In some cases, it may be desirable to not have the backplane PCI reset cause a board reset.

The RESET_OUT_L pin of the IXP2400 is connected to the FPGA and the PM3386/7 Ethernet Controllers. This allows software to independently reset these devices via the EXRST bit in the IXP_RESET0 register without causing all PCI devices to be reset.

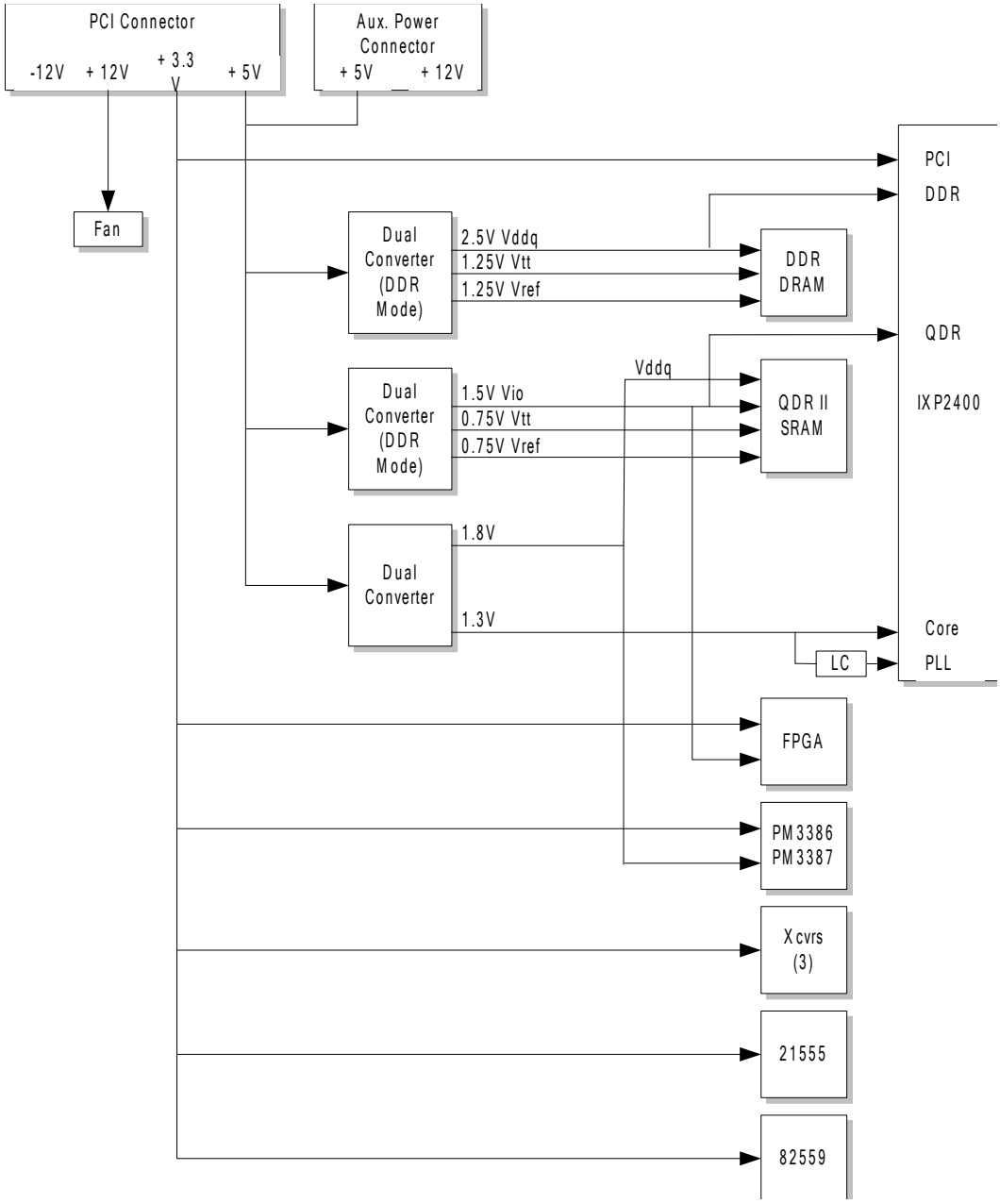
The CFG_BOOT_PROM pin is strapped to force the IXP2400 to boot from its Flash ROM. This causes the Flash ROM device to be mapped into location 0x0, and the IXP2400 starts execution of code from the Flash ROM. Once execution from the Flash ROM code is no longer necessary, the code can make DRAM appear at 0x0 by setting the FLASH_ALIAS_DISABLE bit in the MISC_CONTROL register.

The CFG_PCI_BOOT_HOST pin is strapped to force the IXP2400 to configure all the devices on the internal PCI bus. The boot code must test this bit in the STRAP_OPTIONS register, and if set, configure all internal PCI devices.

Power

The next figure shows the a block diagram of the ENP-2611's power generation subsystem.

Figure 3-3. Power Subsystem



As shown in the previous figure, power for the ENP-2611 devices is derived from the +5V and +3.3V supplies provided by on the PCI backplane connector. Many internal power rails are needed to supply the various components on the board. These are all derived from the +5V and +3.3V input voltages. +12V is used only to power the cooling fan for the IXP2400 processor. –12V is unused.

Table 3-3. Maximum Power Table

Supply	Current	Watts
+3.3V	2.5A	8.25 W
+5V	3.1A	15.5 W
+12V	100 mA	1.2 W
–12V	Not used	Not used

Note: Typical Operating power is 20–25 Watts.

+2.5V and +1.25V DDR SDRAM Supply

A multi-mode dual synchronous PWM switching regulator is used to generate the +2.5V V_{DDQ} and +1.25V V_{TT} termination voltage required by the DDR SDRAM circuitry. This regulator is operated in "DDR Mode" in which the +1.25V termination voltage is generated from the +2.5V output, and thereby tracking V_{DDQ} /2.

Overvoltage protection prevents the output from exceeding 120% of the set point, and undervoltage protection turns off the output when it drops below 75% of the set value after softstart has completed. An overcurrent function monitors the voltage drop across the lower FET.

The regulator operates from the +5V input voltage.

+1.5V and +0.75V QDR SRAM Supply

A multi-mode dual synchronous PWM switching regulator is used to generate the +1.5V V_{IO} and +0.75V V_{TT} termination voltage required by the QDR SRAM circuitry. This regulator is operated in "DDR Mode" in which the +0.75V termination voltage is generated from the +1.25V output, and thereby tracking V_{IO} /2.

Overvoltage protection prevents the output from exceeding 120% of the set point, and undervoltage protection turns off the output when it drops below 75% of the set value after softstart has completed. An overcurrent function monitors the voltage drop across the lower FET.

The regulator operates from the +5V input voltage.

+1.3V IXP2400 Core Supply

One channel of a multi-mode dual synchronous PWM switching regulator is used to generate the +1.3V core voltage required by the IXP2400. This regulator is operated in "Dual Mode" in which each half of the controller operates independently from the other.

Overvoltage protection prevents the output from exceeding 120% of the set point, and undervoltage protection turns off the output when it drops below 75% of the set value after softstart has completed. An overcurrent function monitors the voltage drop across the lower FET.

The regulator operates from the +5V input voltage.

+1.8V Miscellaneous Supply

The second channel of a multi-mode dual synchronous PWM switching regulator is used to generate the +1.8V voltage required by the QDR SRAM V_{DDQ} and the PM3386/7 Ethernet controllers. This regulator is operated in "Dual Mode" in which each half of the controller operates independently from the other.

Overvoltage protection prevents the output from exceeding 120% of the set point, and undervoltage protection turns off the output when it drops below 75% of the set value after softstart has completed. An overcurrent function monitors the voltage drop across the lower FET.

The regulator operates from the +5V input voltage.

Power Supply Sequencing

Per Intel recommendations, power-sequencing circuitry on the ENP-2611 ensures the power supplies are energized in the following order. The delay between each one is 5 mS or less.

1. The +3.3V supply is brought up before the +1.3V supply.
2. The +1.3V Core and PLL supply is brought up before the +1.5V and +2.5V supplies.
3. The +2.5V DDR supply is brought up before or at the same time as the +1.25V supply.
4. The +1.5V QDR supply is brought up before or at the same time as the +0.75V supply.

During power-down, all power supplies are brought down simultaneously.

PCI Device Configuration

The PCI peripherals' configuration spaces are accessed with the parameters in the following table. Please refer to the device documentation for details regarding the Configuration Space registers.

Table 3-4. PCI Device Configuration

Peripheral	IDSEL	Bus #	Device #	Function #	PCI INT #	PCI Arb. (REQ/GNT)
IXP2400	AD16	0 (Local64)	0	0	A	N/A (Arbiter)
21555 PCI/PCI Bridge	AD17	0 (Local64)	1	0	B	0

Table 3-4. PCI Device Configuration

Peripheral	IDSEL	Bus #	Device #	Function #	PCI INT #	PCI Arb. (REQ/GNT)
PCI2050B PCI/PCI Bridge	AD20	0 (Local64)	4	0	N/A	1
82559 Ethernet	AD16	1 (Local32)	0	0	A	0
SPI-3 Option Board	AD17	1 (Local32)	1	0	B	1

1 After reset, Flash ROM appears at 00000000h until disabled by software writing to Flash_Alias_Disable bit.

2 FPGA SPI-3 Bridge registers are defined in *Appendix D, SPI-3 Bridge register definitions*.

Thermal Design

The IXP2400 has a maximum power dissipation of 16 watts (13 W typical). Heat produced by the processor is dissipated with a low-profile aluminum fan/heatsink assembly attached to the top of the PBGA package.. This is similar to the cooling solution used on AGP graphics cards. The fan operates from the +12V input supply.

When installed in a standard PC, especially a tower chassis, there may not be enough airflow to adequately cool the ENP-2611. For more information, see *Environmental Specifications* on page 5.

A IXP2400 Memory Map

Table 3-5. IXP2400 memory map

Range		Content
0 to 2GB	00000000-7FFFFFFF	DRAM, XScale Flash ROM [1]
	00000000-07FFFFFF	128MB DRAM populated
	00000000-0FFFFFFF	256MB DRAM populated
	00000000-1FFFFFFF	512MB DRAM populated
	00000000-3FFFFFFF	1GB DRAM populated
	00000000-7FFFFFFF	2GB DRAM populated
2GB to 3GB	80000000-8FFFFFFF	SRAM Channel 0
	90000000-9FFFFFFF	SRAM Channel 1
	A0000000-AFFFFFFF	SRAM Channel 2 (IXP2800 only)
	B0000000-BFFFFFFF	SRAM Channel 3 (IXP2800 only)
3GB to 3.5GB	C0000000-C000FFFF	Scratchpad CSRs
	C0004000-C0004FFF	CAP Fast Write CSRs
	C0004800-C00048FF	CAP Scratchpad Memory CSRs
	C0004900-C000491F	CAP Hash Unit Multiplier Registers
	C0004A00-C0004A1F	CAP IXP Global CSRs
	C000C000-C000CFFF	Microengine CSRs
	C0010000-C001FFFF	CAP XScale GPIO Registers
	C0020000-C002FFFF	CAP XScale Timer CSRs
	C0030000-C003FFFF	CAP XScale UART Registers
	C0050000-C005FFFF	PMU?
	C0080000-C008FFFF	CAP XScale Slow Port CSRs
	C4000000-C4FFFFFF	XScale Flash ROM (Chip-select 0) (16MB 28F128J3)
	C5000000-C53FFFFF	FPGA SPI-3 Bridge Registers (Chip-select 0)[2]
	C5800000	POST Register (Chip-select 0)
	C5800004	Port 0 Transceiver Register (Chip-select 0)
	C5800008	Port 1 Transceiver Register (Chip-select 0)

Table 3-5. IXP2400 memory map

Range		Content
3GB to 3.5GB (cont'd)	C580000C	Port 2 Transceiver Register (Chip-select 0)
	C5800010	FPGA Programming Register (Chip-select 0)
	C5800014	FPGA Load Port (Chip-select 0)
	C5800018	Board Revision Register (Chip-select 0)
	C580001C	CPLD Revision Register (Chip-select 0)
	C5800020-C5FFFFFF	Unused (Chip-select 0)
	C6000000-C63FFFFF	PM3386 #0 Registers (Chip-select 1)
	C6400000-C67FFFFF	PM3387 #1 Registers (Chip-select 1)
	C6800000-CBFFFFFF	Unused (Chip-select 1)
	C6C00000-CFFFFFFF	SPI-3 Option Board (Chip-select 1)
	C7000000-C7FFFFFF	Unused (Chip-select 1)
	C8000000-C8003FFF	Media and Switch Fabric (MSF) Registers
	CA000000-CBFFFFFF	Scratchpad Memory
	CC000100-CC0001FF	SRAM Channel 0 Queue Array CSRs
	CC010000-CC0101FF	SRAM Channel 0 CSRs
	CC400100-CC4001FF	SRAM Channel 1 Queue Array CSRs
	CC410100-CC4101FF	SRAM Channel 1 CSRs
	CC800100-CC8001FF	SRAM Channel 2 Queue Array CSRs (IXP2800 only)
	CC810100-CC8101FF	SRAM Channel 2 CSRs (IXP2800 only)
	CCC00100-CCC001FF	SRAM Channel 3 Queue Array CSRs (IXP2800 only)
	CCC10100-CCC101FF	SRAM Channel 3 CSRs (IXP2800 only)
	CE000000-CEFFFFFF	SRAM Channel 0 Ring CSRs
	CE400000-CE4FFFFF	SRAM Channel 1 Ring CSRs
	CE800000-CE8FFFFF	SRAM Channel 2 Ring CSRs (IXP2800 only)
	CEC00000-CECFFFFF	SRAM Channel 3 Ring CSRs (IXP2800 only)
	D0000000-D000003F	DRAM Channel 0 CSRs
	D0000040-D000007F	DRAM Channel 1 CSRs (IXP2800 only)
	D0000080-D00000BF	DRAM Channel 2 CSRs (IXP2800 only)
	D6000000-D6FFFFFF	XScale Interrupt Controller CSRs

Table 3-5. IXP2400 memory map

Range		Content
3GB to 3.5GB (cont'd)	D7000220-D700022F	XScale Breakpoint CSRs
	D7004900-D700491F	XScale Hash Unit Operand/Result CSRs
	D8000000-D8FFFFFF	PCI I/O Space Commands
	DA000000-DAFFFFFF	PCI Configuration Type 0 Commands
	DB000000-DBFFFFFF	PCI Configuration Type 1 Commands
	DC000000-DDFFFFFF	PCI Special and IACK Commands
	???	System Control Coprocessor (CP15)
	???	Coprocessor 14 (CP14)
	DE000000-DEFFFFFF	IXP PCI Configuration Space CSRs
	DF000000-DF00015F	PCI CSRs
3.5GB to 4GB	E0000000-FFFFFFFF	PCI Memory Space Commands

1 After reset, Flash ROM appears at 00000000h until disabled by software writing to Flash_Alias_Disable bit.

2 FPGA SPI-3 Bridge registers are defined in the *Appendix D, SPI-3 Bridge register definitions*.

B Registers

The following memory-mapped registers reside in the CPLD.

FPGA Registers (C5000000h – C57FFFFFh)

The SPI-3 FPGA is configured through 8-bit registers in this address space. For register descriptions, please refer to *Appendix D, SPI-3 Bridge register definitions*.

POST Register (C5800000h)

7	6	5	4	3	2	1	0
POST Register							

Bits 7–0 The hex value written to this register displays on the RadiSys Mini-POST board installed in the POST header. The Mini-POST board converts the hex value to a BCD value and displays it.
When read, the register reflects the last value written.
This register is cleared to 00h on power-up and reset.

Port 0, 1, 2 Transceiver Registers (C5800004h, C5800008h, C580000Ch)

7	6	5	4	3	2	1	0
Reserved	MOD_IN~	TX_FAULT	LOS	USER	Reserved	SDA	SCL

Bit 6 MODule INstalled
This read-only bit reflects the Mod Def 0 output of the transceiver.

0 The transceiver module is installed.

1 The module is not installed.

Bit 5 Transmitter FAULT
This read-only bit reflects the TX_FAULT output of the transceiver.

0 The transmitter is operating normally.

1 Either the transciever module is not installed, or the transmitter safety circuitry detected an error.

Bit 4 Loss Of Signal
This read-only bit reflects the LOS output of the transceiver.

0 The link at the receiver is operating properly.

1 The link is operating outside the values required for proper operation. This may be due to uninstalled or broken cables, or a disabled, failing, or powered-off transmitter on the far end of the cable.

Bit 3 USER LED (non-MP versions only)
This read/write bit controls the state of the USER LED on the front bracket.

0 The USER LED is not lit. Powerup and reset clears this bit to 0.

1 The USER LED is lit. When read, the bit reflects the last value written.

Bit 1 Serial DAta
This read/write bit connects to the SDA (Mod Def 2) pin on the transceiver. It is used to read back the data contained within the EEPROM on the transceiver.

1 The SDA pin is tri-stated and allowed to be pulled high. It is set to 1 on powerup and reset.

0 The SDA pin is driven low. When read, this bit reflects the current state of the SDA pin.

Bit 0 Serial CLock
This read/write bit controls the SCL (Mod Def 1) pin on the transceiver.

1 The SCL pin is tri-stated and allowed to be pulled high. It is set to 1 on powerup and reset.

0 The SCL pin is driven low. When read, this bit reflects the current state of the SCL pin.

FPGA Programming Register (C5800010h)

7	6	5	4	3	2	1	0
Reserved	Reserved	INIT~	DONE	Reserved	Reserved	Reserved	PROG

This register controls loading of the on-board FPGA. After power-up, or to change the internal code, the FPGA must be loaded by the IXP2400. This is done through the Slow Port, via the FPGA's parallel port asynchronous (PPA) mode. The reload process is started by setting the PROG bit. The FPGA data is loaded through 8-bit writes. Load progress is monitored using the INIT and DONE signals. For more information on using a parallel port to load the FPGA, refer to the Xilinx Virtex II data sheet.

Bit 5 INIT~
This read-only bit reflects the state of the INIT~ pin on the FPGA. 0 indicates a start of the configuration process.

Bit 4 DONE
This read-only bit reflects the state of the DONE pin on the FPGA. 0 indicates FPGA initialization is not complete.

Bit 0 PROG
This read/write bit is used to start the initialization process. Setting this bit to 1 starts FPGA load process.
It is cleared to 0 on powerup and reset, and when INIT goes true.

FPGA Load Port Register (C5800014h)

7	6	5	4	3	2	1	0
FPGA Load Port Register							

This register loads data into the on-board FPGA. After power-up, or to change the internal code, the FPGA must be loaded by the IXP2400. This is done through the Slow Port, via the FPGA's parallel port asynchronous (PPA) mode. The reload process is started by setting the PROG bit in the FPGA Programming Register above. The FPGA data is loaded through 8-bit writes to this port. Load progress is monitored using the INIT and DONE signals in the FPGA Programming Register. For more information on using a parallel port to load the FPGA, refer to the Xilinx Virtex II data sheet

Board Revision Register (C5800018h)

7	6	5	4	3	2	1	0
FL_WREN	Reserved	Reserved	BRD_ID			BRD_REV	

This read-only register determines the identity and revision of the ENP-2611. All unused bits return 0.

Bit 7 FLash_WRite ENable
This read-only bit reflects the state of the Flash write-enable jumper. 0 indicates the jumper is placed in the Disable position, and the flash cannot be written. 1 indicates the jumper is placed in the Enable position, and the flash may be written.

Bits 6–5 These bits are reserved, and return a 0 when read.

Bits 4–2 BoaRD_Identity
000 = Unused
001 = PFS-283/ENP-2611
010 – 111 = Reserved

Bits 1–0 BoaRD_REVision
This value increments each time the PCB (raw fab) is revised. The first version is 00.

CPLD Revision Register (C580001Ch)

7	6	5	4	3	2	1	0
CPLD Revision Register							

This read-only register determines the revision of the CPLD on the ENP-2611. It contains a hexadecimal value on starting from the LSB which contains the CPLD revision. All unused bits return 0.

IXP2400 GPIO Pin Assignments

The GPIO pins of the IXP2400 are used as follows.

GPIO Pins

GPIO pin function	7	6	5	4	3	2	1	0
Power-up	Unused	CFG_PCI_SWIN		CFG_PCI_DWIN		CFG_ PCI_ARB	CFG_PCI_ BOOT_ HOST	CFG_ BOOT_ PROM
Normal operation	SCL	SDA	Unused	THERM_I NT~	OB_ INT~	FPGA_ INT~	ENET1_IN T~	ENET0_IN T~

Pin description

GPIO7 Power-up: Unused
Normal Operation: Serial CLock
This read/write bit controls the SCL clock signal on the serial bus, which contains the EEPROM SPD on the SODIMM, and the thermal diode temperature monitor for the IXP2400.

GPIO6, 5 Power-up: ConFiGure PCI SRAM WINdow
On powerup, the PCI SRAM window size is set to the value indicated below. These inputs are connected to the DIP switches.

00 = SRAM BAR size is 32 MB

01 = SRAM BAR size is 64 MB

10 = SRAM BAR size is 128 MB

11 = SRAM BAR size is 256 MB

Normal Operation:
GPIO6 = Serial DAta
This read/write bit controls the SDA data signal on the serial bus, which contains the EEPROM SPD on the SODIMM, and the thermal diode temperature monitor for the IXP2400. It is used to read back the data contained within the these devices.
GPIO5 = Unused

GPIO4, 3 Power-up: ConFiGure PCI DRAM WINdow
On powerup, the PCI DRAM window size is set to the value indicated below. These inputs are connected to the DIP switches.

00 DRAM BAR size is 128 MB

01 DRAM BAR size is 256 MB

10 DRAM BAR size is 512 MB

11 DRAM BAR size is 1024 MB

Normal Operation:
GPIO4 = THERMal INTerrupt
This pin is also used as the interrupt input from the IXP2400 thermal diode temperature sensor. It should be set to a level-sensitive low-true interrupt pin during initialization.
GPIO3 = Option Board INTerrupt

This pin is also used as the interrupt input from the SPI-3 Option Board, if needed. It should be set to a level-sensitive low-true interrupt pin during initialization.

GPIO2 Power-up: ConFiGure PCI ARBiter

0 IXP2400 do not perform the PCI arbitration function.

1 IXP2400 do the PCI arbitration function. The ENP-2611 is hardwired to this mode.

Normal Operation: FPGA_INT~
This pin is also used as the interrupt input from the FPGA, which handles all of the devices on the POS-PHY channels. It should be set to a level-sensitive low-true interrupt pin during initialization.

GPIO1 Power-up: ConFiGure PCI BOOT HOST

0 The XScale core do not configure the system.

1 The XScale core does configure the system. The ENP-2611 is hardwired to this mode.

Normal Operation: ENET1_INT~
This pin is also used as the interrupt input from the PM3387 #1, which handles the Port 2 Ethernet channel. It should be set to a level-sensitive low-true interrupt pin during initialization.

GPIO0 Power-up: ConFiGure PROM BOOT

0 The XScale core boots from DRAM initialized by the backplane PCI Host.

1 The XScale core boots from Flash PROM. The ENP-2611 is hardwired to this mode.

Normal Operation: ENET0_INT~
This pin is also used as the interrupt input from the PM3386 #0, which handles the Port 0 and 1 Ethernet channels. It should be set to a level-sensitive low-true interrupt pin during initialization.

C Connectors

This appendix details the connectors on the ENP-2611 CPU board and gives the signal pinout of each connector.

This product includes the connectors listed in the table below. When reading this file online, you can immediately view information about any connector by placing the mouse cursor over a connector name and clicking:

For information about...	Go to this page...
Connector locations	54
PCI connector	55
Ethernet SFP connectors	58
Indicator LEDs	59
SPI-3 Option Board Connector	59
Debug	60
Reset switch	60
Debug Ethernet connector	60
Debug Serial Port Header	61
Null-modem serial cable	61

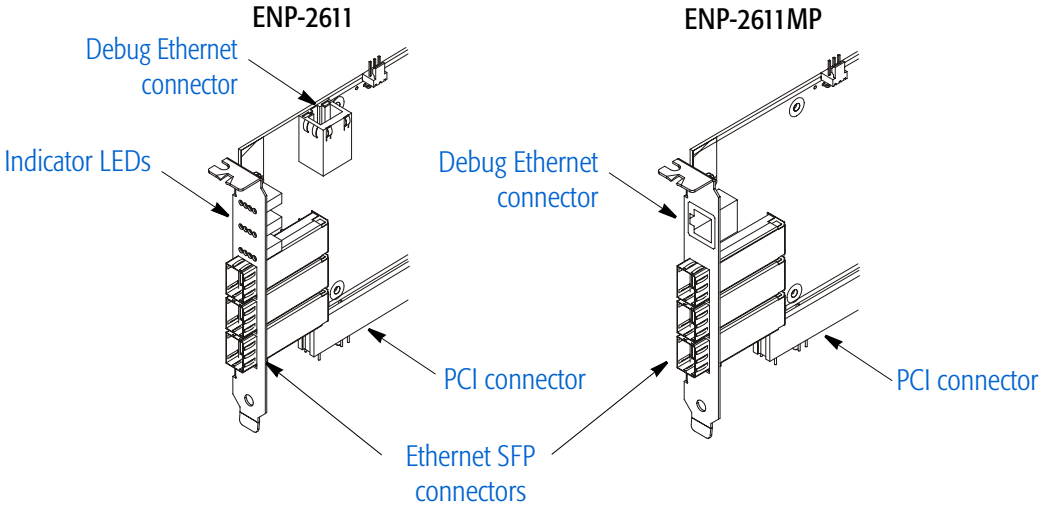
Connector locations

The next figure shows the locations of the connectors on the ENP-2611.

Note

For information about installation, see *Chapter 2, Installation and configuration*.

Figure C-1. Connector locations



PCI connector

The PCI bus card edge connector used on the ENP-2611 mates with a Universal 64-bit PCI bus connector in a host chassis. This connector complies with the *PCI Local Bus Specification Revision 2.3*.

All GND fingers are connected to the digital ground of the ENP-2611. All voltage fingers (-12V, +12V, +5V, +3.3V, and $+V_{I/O}$ are capacitively coupled to the nearest voltage plane in the Z axis, providing an AC signal return path for the backplane signals.

Table C-1. PCI Bus Connector

Solder Side Signal Name	Pin	Pin	Component Side Signal Name
-12V	B01	A01	TRST#
TCK	B02	A02	+12V
GND	B03	A03	TMS
TDO	B04	A04	TDI
+5V	B05	A05	+5V
+5V	B06	A06	INTA#
INTB#	B07	A07	INTC#
INTD#	B08	A08	+5V
PRSNT1#	B09	A09	Reserved
Reserved	B10	A10	$+V_{I/O}$
PRSNT2#	B11	A11	Reserved
Keyway			Keyway
Keyway			Keyway
Reserved	B14	A14	+3.3V AUX
GND	B15	A15	RST#
CLK	B16	A16	$+V_{I/O}$
GND	B17	A17	GNT#
REQ#	B18	A18	GND
$+V_{I/O}$	B19	A19	PME#
AD31	B20	A20	AD30
AD29	B21	A21	+3.3V
GND	B22	A22	AD28
AD27	B23	A23	AD26
AD25	B24	A24	GND
+3.3V	B25	A25	AD24
C/BE3#	B26	A26	IDSEL
AD23	B27	A27	+3.3V
GND	B28	A28	AD22
AD21	B29	A29	AD20
AD19	B30	A30	GND
+3.3V	B31	A31	AD18
AD17	B32	A32	AD16

Table C-1. PCI Bus Connector

Solder Side Signal Name	Pin	Pin	Component Side Signal Name
C/BE2#	B33	A33	+3.3V
GND	B34	A34	FRAME#
IRDY#	B35	A35	GND
+3.3V	B36	A36	TRDY#
DEVSEL#	B37	A37	GND
PCIXCAP	B38	A38	STOP#
LOCK#	B39	A39	+3.3V
PERR#	B40	A40	SMBCLK
+3.3V	B41	A41	SMBDAT
SERR#	B42	A42	GND
+3.3V	B43	A43	PAR
C/BE1#	B44	A44	AD15
AD14	B45	A45	+3.3V
GND	B46	A46	AD13
AD12	B47	A47	AD11
AD10	B48	A48	GND
M66EN	B49	A49	AD09
Keyway			Keyway
Keyway			Keyway
AD08	B52	A52	C/BE0#
AD07	B53	A53	+3.3V
+3.3V	B54	A54	AD06
AD05	B55	A55	AD04
AD03	B56	A56	GND
GND	B57	A57	AD02
AD01	B58	A58	AD00
$+V_{I/O}$	B59	A59	$+V_{I/O}$
ACK64#	B60	A60	REQ64#
+5V	B61	A61	+5V
+5V	B62	A62	+5V
Keyway			Keyway
Keyway			Keyway
Reserved	B63	A63	GND
GND	B64	A64	C/BE7#
C/BE6#	B65	A65	C/BE5#
C/BE4#	B66	A66	$+V_{I/O}$
GND	B67	A67	PAR64
AD63	B68	A68	AD62
AD61	B69	A69	GND
$+V_{I/O}$	B70	A70	AD60

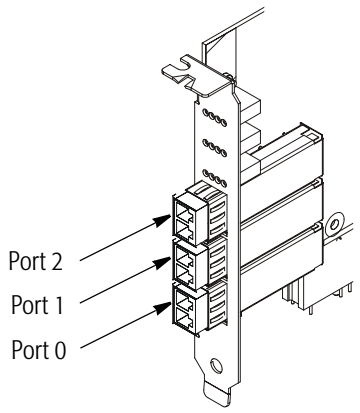
Table C-1. PCI Bus Connector

Solder Side Signal Name	Pin	Pin	Component Side Signal Name
AD59	B71	A71	AD58
AD57	B72	A72	GND
GND	B73	A73	AD56
AD55	B74	A74	AD54
AD53	B75	A75	$+V_{I/O}$
GND	B76	A76	AD52
AD51	B77	A77	AD50
AD49	B78	A78	GND
$+V_{I/O}$	B79	A79	AD48
AD47	B80	A80	AD46
AD45	B81	A81	GND
GND	B82	A82	AD44
AD43	B83	A83	AD42
AD41	B84	A84	$+V_{I/O}$
GND	B85	A85	AD40
AD39	B86	A86	AD38
AD37	B87	A87	GND
$+V_{I/O}$	B88	A88	AD36
AD35	B89	A89	AD34
AD33	B90	A90	GND
GND	B91	A91	AD32
Reserved	B92	A92	Reserved
Reserved	B93	A93	GND
GND	B94	A94	Reserved

Ethernet SFP connectors

These connectors, located on the front panel, provide support for one gigabit Ethernet channel apiece:

Figure C-2. Gigabit ports



The three 1000Base-SX Ethernet interfaces use 20-pin right-angle MSA-compliant connectors. They are surrounded by a metal shield connected to the Shield plane of the board which is connected to chassis ground through the front panel bracket. The metal shield has a 1 degree tilt which elevates the open end to comply with the PCI mechanical specification, and protrudes through the rear bracket. MSA-compliant SFP modules slide into the metal shield and plug into the connector. The modules have LC type fiber receptacles that accept 50 um or 62.5 um multimode fiber cables with LC connectors or RJ-45 receptacles that accept CAT-5 copper cables with RJ-45 connectors.

Table C-2. Gigabit SFP Ethernet Connectors

Pin	Description	Pin	Description
1	$V_{EE}T$	20	$V_{EE}T$
2	TX_FAULT	19	TD-
3	TX_DISABLE	18	TD+
4	MOD-DEF2	17	$V_{EE}T$
5	MOD-DEF1	16	$V_{CC}T$
6	MOD-DEF0	15	$V_{CC}T$
7	RATE_SELECT	14	$V_{EE}R$
8	LOS	13	RD+
9	$V_{EE}R$	12	RD-
10	$V_{EE}R$	11	$V_{EE}R$

Indicator LEDs

Two banks of four right-angle LEDs. one bank for each channel, are located above the transceivers and are visible through the rear bracket on the non-MP version. For more information about these LEDs, see *Gigabit Ethernet Channels* on page 26.

The transceivers, the PM3386/7 Ethernet Controllers, and the LED Registers of the CPLD each provide some status information to drive these LEDs.

Figure C-2. LEDs

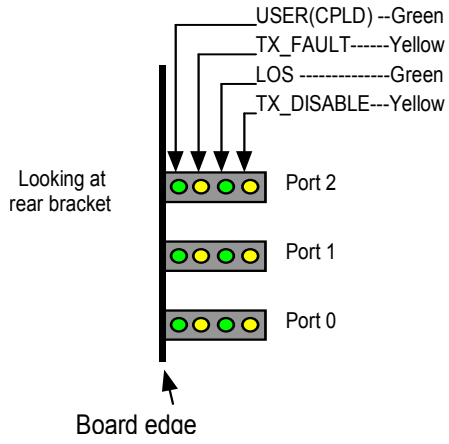


Table C-3. LED signals

LED	Color	Status	Description
TX_DISABLE	Yellow	Lit	The transceiver is disabled via the TXEN bit in the respective EGMACn PM3386's GMACC1 register.
		Not lit	Normal operation.
TX_FAULT (Driven by an output of the transceiver)	Yellow	Lit	The transceiver is not installed, or a fault is detected by the transmitter safety circuitry.
		Not lit	Normal operation.
LOS (Loss Of Signal) (A transceiver output)	Green	Lit	A proper link is established.
		Not lit	The link is outside the required values for proper operation.
USER	Green	Lit	The corresponding bit of the transceiver register in the CPLD is set.
		Not lit	The corresponding bit of the transceiver register in the CPLD is cleared.

SPI-3 Option Board Connector

A 10x40 position 0.050" pitch female BGA connector provides expansion to a future proprietary SPI-3 Option Board. The connector is installed on the back side of the board. The Option Boards are stacked at 0.8" pitch to allow their interface connectors to protrude through the rear panel in the PCI slot behind the ENP-2611. If the Option

Board is unused, a shorting board with a mating Samtec YFT-40-05-G-10-SB-TR male connector must be installed.

Debug

Reset switch

A right-angle momentary pushbutton reset switch is located on the top edge of the board. When depressed, it causes a hard reset to be asserted to the IXP2400, which in turn causes all of the internal peripherals on the board to be reset. The reset switch is conditioned by a micro-monitor, which lengthens the reset pulse to the required duration.

Debug Ethernet connector

A 10Base-T/100Base-TX shielded RJ45 Ethernet connector is mounted on the top edge of the board, and is used for debug only. The metal shield of the connector is connected to chassis ground through the front panel bracket. The connector has built-in LEDs which indicate Ethernet Link Status and Activity. The "LINK" LED is green for a 10 Mb link and amber for a 100 Mb link. The pins noted as "AC-term" are connected through 75 ohm resistors to a common net, which is AC coupled to chassis ground.

Figure C-3. Debug Ethernet connector (J1/MP version)or J2/non-MP version)

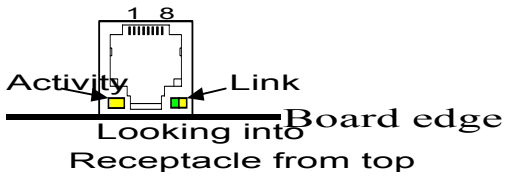


Table C-4. Debug Ethernet connector

Pin	Description	Pin	Description
1	Transmit +	5	AC term
2	Transmit –	6	Receive –
3	Receive +	7	AC term
4	AC term	8	AC term

Debug Serial Port Header

A 1x3, 0.1" right-angle keyed male header with friction lock is provided which can be used for connection of a serial cable to the UART of the IXP2400.

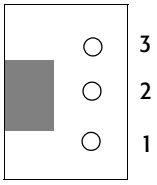
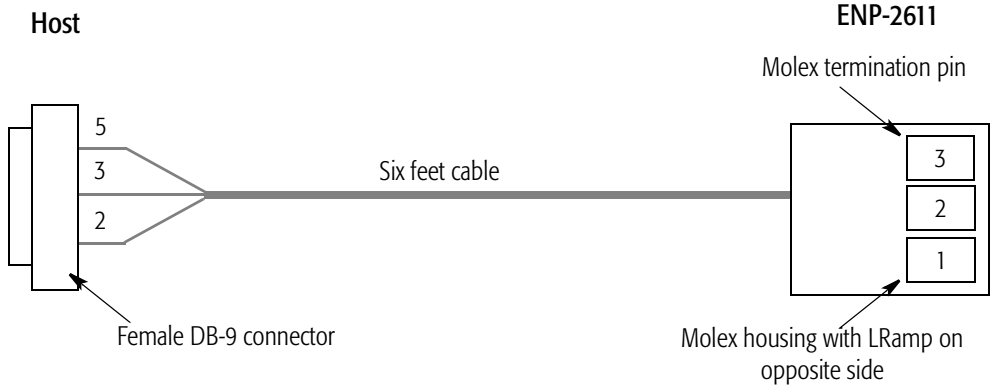


Table C-5. Debug Serial Port header (J3)

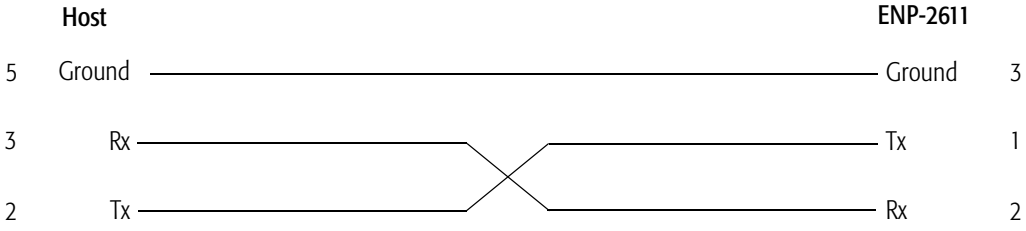
Pin	Description
1	Transmit Data (TXD)
2	Receive Data (RXD)
3	GND

Null-modem serial cable

The next figure shows the custom serial cable shipped with the board. This cable is configured as a null-modem connection.



Electrical connections



Flash Programming header

A 1x3-pin jumper that you use to specify the Flash programming mode:

Figure C-4. Flash Programming header settings

Disables Flash programming

Enables Flash programming

⚠ CAUTION

Leave this jumper in the default position. Other positions cause the boot to fail.

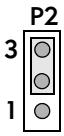


Table C-6. Flash Programming header

Pin	Signal
1	N/C
2	FL_WREN
3	+3.3V

D SPI-3 Bridge register definitions

This appendix defines the SPI Bridge registers.

Table D-1. Configuration registers

Address offset	Register Symbol	Register Name	Access
00h	IDLO Byte	SPI-3 Bridge identification low	RO
01h	IDHI	SPI-3 Bridge identification high byte	RO
02h	RID	Revision identification	RO
03h	RESET	Reset Control register	R/W
04h	INTREN0	Interrupt enable 0	R/W
05h	INTREN1	Interrupt enable 1	R/W
06h	INTRSTAT0	Interrupt status 0	R/WC
07h	INTRSTAT1	Interrupt status 1	R/WC
08h	PORTEN	Port enable	R/W
09h	BURST	Burst size	R/W
0Ah	PORTPAUS	Port PAUSE	R/W
0Bh	PORTPAUSD	Port PAUSED	RO
0Ch		Reserved	RO
0Dh		Reserved	RO
0Eh		Reserved	RO
0Fh		Reserved	RO
10h	PHY0RX	PHY0 RX FIFO Control	R/W
11h	PHY1RX	PHY1 RX FIFO Control	R/W
12h	PHY0TX	PHY0 TX FIFO Control	R/W
13h	PHY1TX	PHY1 TX FIFO Control	R/W
14h		Reserved	RO
15h	IXPRX HI CNTR	IXP RX Counter High	RO
16h	PHY0RX HI CNTR	PHY0 RX Counter High	RO
17h	PHY1RX HI CNTR	PHY0 RX Counter High	RO
18h	IXPRX CNTR	IXP RX Counter	RO
19h	PHY0RX CNTR	PHY0 RX Counter	RO
1Ah	PHY1RX CNTR	PHY1 RX Counter	RO
1Bh	IXPTX CNTR	IXP TX Counter	RO
1Ch	PHY0TX CNTR	PHY0 TX Counter	RO
1Dh	PHY1TX CNTR	PHY1 TX Counter	RO
1Eh	DEBUG0	Debug Register 0	R/W
1Fh	DEBUG1	Debug Register 1	R/W

Table D-2. Access definitions

Access type	Definition
WO	Write Only. Reads to this register return zero.
RO	Read Only. Writes to this register or bit have no effect.
R/W	Read / Write. Capability to read and write this register or bit normally.
R/WC	Read / Write Clear. This register or bit can only be set by hardware.Software can clear a bit by writing a 1 to that bit. Software can clear an entire register by writing 8'hFF to that register. Writing a 0 or writing a 1 to a bit that has not been set by hardware has no effect.

IDLO, SPI-3 Bridge Identification Low Byte: A=00h, R=31h

Bit	Access	Description
7:0	RO	SPI-3 Bridge Identification register. This is hardwired to the low byte of the Radisys PCI vendor ID: 31h.

IDHI, SPI-3 Bridge Identification High Byte: A=01h, R=13h

Bit	Access	Description
7:0	RO	SPI-3 Bridge Identification register. This is hardwired to the high byte of the Radisys PCI vendor ID: 13h.

RID, Revision Identification: A=02h, R=00h

Bit	Access	Description
7:0	RO	Revision Identification register. SPI-3 Bridge revision ID. This value increments with each FPGA revision.

RESET, Reset Control Register: A=03h, R=00h

Bit	Access	Description
7:2	RO	Hardwired to 0.
1	WO	Global Reset. When this bit is loaded to a 1, the SPI-3 Bridge is internally reset, including configuration registers. Wait 5 clocks of the slowest frequency clock after causing a global reset before accessing the bridge.
0	WO	Logic Reset. When this bit is loaded to a 1, the SPI-3 Bridge logic is internally reset, excluding configuration registers. Wait 5 clocks of the slowest frequency clock after causing a logic reset before accessing the bridge.

INTREN0, Interrupt Enable 0: A=04h, R=00h

Bit	Access	Description
7	R/W	phy1, channel 1, tx fifo overflow interrupt enable. Enables an interrupt to occur when the IXP overflows the phy1, channel 1, tx fifo.
6	R/W	phy1, channel 0, tx fifo overflow interrupt enable. Enables an interrupt to occur when the IXP overflows the phy1, channel 0, tx fifo.
5	R/W	phy0, channel 1, tx fifo overflow interrupt enable. Enables an interrupt to occur when the IXP overflows the phy0, channel 1, tx fifo.

Bit	Access	Description
4	R/W	phy0, channel 0, tx fifo overflow interrupt enable. Enables an interrupt to occur when the IXP overflows the phy0, channel 0, tx fifo.
3	R/W	phy1, channel 1, rx fifo overflow interrupt enable. Enables an interrupt to occur when the PHY1 overflows the phy1, channel 1, rx fifo.
2	R/W	phy1, channel 0, rx fifo overflow interrupt enable. Enables an interrupt to occur when the PHY1 overflows the phy1, channel 0, rx fifo.
1	R/W	phy0, channel 1, rx fifo overflow interrupt enable. Enables an interrupt to occur when the PHY0 overflows the phy0, channel 1, rx fifo.
0	R/W	phy0, channel 0, rx fifo overflow interrupt enable. Enables an interrupt to occur when the PHY0 overflows the phy0, channel 0, rx fifo.

INTREN1, Interrupt Enable 1: A=05h, R=00h

Bit	Access	Description
7	RO	Reserved. Hardwired to 0.
6	RO	Reserved. Hardwired to 0.
5	RO	Reserved. Hardwired to 0.
4	RO	Reserved. Hardwired to 0.
3	RO	Reserved. Hardwired to 0.
2	R/W	phy1 rx parity error interrupt enable. Enables an interrupt to occur when a parity error occurs on the PHY1 RX data bus.
1	R/W	phy0 rx parity error interrupt enable. Enables an interrupt to occur when a parity error occurs on the PHY0 RX data bus.
0	R/W	ixp tx parity error interrupt enable. Enables an interrupt to occur when a parity error occurs on the IXP TX data bus.

INTRSTAT0, Interrupt Status 0: A=06h, R=00h

Bit	Access	Description
7	R/WC	phy1, channel 1, tx fifo overflow. The IXP overflowed the phy1, channel 1, tx fifo.
6	R/WC	phy1, channel 0, tx fifo overflow. The IXP overflowed the phy1, channel 0, tx fifo.
5	R/WC	phy0, channel 1, tx fifo overflow. The IXP overflowed the phy0, channel 1, tx fifo.
4	R/WC	phy0, channel 0, tx fifo overflow. The IXP overflowed the phy0, channel 0, tx fifo.
3	R/WC	phy1, channel 1, rx fifo overflow. The PHY1 overflowed the phy1, channel 1, rx fifo.
2	R/WC	phy1, channel 0, rx fifo overflow. The PHY1 overflowed the phy1, channel 0, rx fifo.
1	R/WC	phy0, channel 1, rx fifo overflow. The PHY0 overflowed the phy0, channel 1, rx fifo.
0	R/WC	phy0, channel 0, rx fifo overflow. The PHY0 overflowed the phy0, channel 0, rx fifo.

INTRSTAT1, Interrupt Status 1: A=07h, R=00h

Bit	Access	Description
7	RO	Reserved. Hardwired to 0.
6	RO	Reserved. Hardwired to 0.
5	RO	Reserved. Hardwired to 0.
4	RO	Reserved. Hardwired to 0.
3	RO	Reserved. Hardwired to 0.
2	R/WC	phy1 rx parity error. A parity error was detected on the phy1 rx interface.
1	R/WC	phy0 rx parity error. A parity error was detected on the phy0 rx interface.
0	R/WC	ixp tx parity error. A parity error was detected on the ixp tx interface.

PORTEN, Port Enable: A=08h, R=00h

Bit	Access	Description
7	R/W	phy1, channel 1, tx fifo enable. When clear blocks the write from the IXP into the phy1 1 txfifo. Transaction completes normally on the IXP SPI-3 TX bus. The transaction is not forwarded to either PHY SPI-3 TX bus.
6	R/W	phy1, channel 0, tx fifo enable. When clear blocks the write from the IXP into the phy1 0 txfifo. Transaction completes normally on the IXP SPI-3 TX bus. The transaction is not forwarded to either PHY SPI-3 TX bus.
5	R/W	phy0, channel 1, tx fifo enable. When clear blocks the write from the IXP into the phy0 1 txfifo. Transaction completes normally on the IXP SPI-3 TX bus. The transaction is not forwarded to either PHY SPI-3 TX bus.
4	R/W	phy0, channel 0, tx fifo enable. When clear blocks the write from the IXP into the phy0 0 txfifo. Transaction completes normally on the IXP SPI-3 TX bus. The transaction is not forwarded to either PHY SPI-3 TX bus.
3	R/W	phy1, channel 1, rx fifo enable. When clear blocks the write from PHY1 into the phy1 1 rxfifo. Transaction completes normally on the PHY1 SPI-3 RX bus. The transaction is not forwarded to the IXP SPI-3 RX bus.

Bit	Access	Description
2	R/W	phy1, channel 0, rx fifo enable. When clear blocks the write from PHY1 into the phy1 0 rxfifo. Transaction completes normally on the PHY1 SPI-3 TX bus. The transaction is not forwarded to the IXP SPI-3 RX bus.
1	R/W	phy0, channel 1, rx fifo enable. When clear blocks the write from PHY0 into the phy0 1 rxfifo. Transaction completes normally on the PHY0 SPI-3 RX bus. The transaction is not forwarded to the IXP SPI-3 RX bus.
0	R/W	phy0, channel 0, rx fifo enable. When clear blocks the write from PHY0 into the phy0 0 rxfifo. Transaction completes normally on the PHY0 SPI-3 RX bus. The transaction is not forwarded to the IXP SPI-3 RX bus.

BURST, Burst Size: A=09h, R=00h

Bit	Access	Description
7:2	RO	Reserved. Hardwired to 0.
1:0	R/W	Burst size. Defines the burst size for SPI-3 transfers. 00b — 16 DWORDs 01b — 32 DWORDs 10b — 64 DWORDs 11b — 16 DWORDs

PORTPAUS, Port Pause: A=0Ah, R=00h

Bit	Access	Description
7:4	RO	Reserved. Hardwired to 0.
3	R/W	phy1 pause[1] signal. Software can control the value of the phy1 pause[1] signal with this register bit.
2	R/W	phy1 pause[0] signal. Software can control the value of the phy1 pause[0] signal with this register bit.
1	R/W	phy0 pause[1] signal. Software can control the value of the phy0 pause[1] signal with this register bit.
0	R/W	phy0 pause[0] signal. Software can control the value of the phy0 pause[0] signal with this register bit.

PORTPAUSD, Port Paused: A=0Bh, R=00h

Bit	Access	Description
7:4	RO	Reserved. Hardwired to 0.
3	RO	phy1 paused[1] signal. Software can read the value of the phy1 paused[1] signal with this register bit.
2	RO	phy1 paused[0] signal. Software can read the value of the phy1 paused[0] signal with this register bit.
1	RO	phy0 paused[1] signal. Software can read the value of the phy0 paused[1] signal with this register bit.
0	RO	phy0 paused[0] signal. Software can control the value of the phy0 paused[0] signal with this register bit.

PHY0RX, PHY0 RX FIFO Control: A=10h, R=00h

<table>
<tr><th>Bit</th><th>Access</th><th>Description</th></tr>
<tr><td>7:0</td><td>R/W</td><td>phy0, channel 1 RX FIFO control.
Tells the bridge how much data needs to be in the phy0 1 rxfifo before phy0 ren is deasserted.
The signal transition occurs just as the FIFO reaches the specified limit regardless of where it is in the packet.
<table><tr><td>0000b</td><td>2 KBytes</td></tr><tr><td>0001b</td><td>1.5 KBytes</td></tr><tr><td>0010b</td><td>1 KBytes</td></tr><tr><td>0011b</td><td>0.5 KBytes</td></tr><tr><td>01xxb</td><td>2 KBytes</td></tr><tr><td>10xxb</td><td>2 KBytes</td></tr><tr><td>11xxb</td><td>2 KBytes</td></tr></table></td></tr>
<tr><td>3:0</td><td>R/W</td><td>phy0, channel 0 RX FIFO control.
Tells the bridge how much data needs to be in the phy0 0 rxfifo before phy0 ren is deasserted.
The signal transition occurs just as the FIFO reaches the specified limit regardless of where it is in the packet.
<table><tr><td>0000b</td><td>2 KBytes</td></tr><tr><td>0001b</td><td>1.5 KBytes</td></tr><tr><td>0010b</td><td>1 KBytes</td></tr><tr><td>0011b</td><td>0.5 KBytes</td></tr><tr><td>01xxb</td><td>2 KBytes</td></tr><tr><td>10xxb</td><td>2 KBytes</td></tr><tr><td>11xxb</td><td>2 KBytes</td></tr></table></td></tr>
</table>

PHY1RX, PHY1 RX FIFO Control: A=11h, R=00h

<table>
<tr><th>Bit</th><th>Access</th><th>Description</th></tr>
<tr><td>7:0</td><td>R/W</td><td>phy1, channel 1 RX FIFO control.
Tells the bridge how much data needs to be in the phy1 1 rxfifo before phy1 ren is deasserted.
The signal transition occurs just as the FIFO reaches the specified limit regardless of where it is in the packet.
<table><tr><td>0000b</td><td>2 KBytes</td></tr><tr><td>0001b</td><td>1.5 KBytes</td></tr><tr><td>0010b</td><td>1 KBytes</td></tr><tr><td>0011b</td><td>0.5 KBytes</td></tr><tr><td>01xxb</td><td>2 KBytes</td></tr><tr><td>10xxb</td><td>2 KBytes</td></tr><tr><td>11xxb</td><td>2 KBytes</td></tr></table></td></tr>
<tr><td>3:0</td><td>R/W</td><td>phy1, channel 0 RX FIFO control.
Tells the bridge how much data needs to be in the phy1 0 rxfifo before phy1 ren is deasserted.
The signal transition occurs just as the FIFO reaches the specified limit regardless of where it is in the packet.
<table><tr><td>0000b</td><td>2 KBytes</td></tr><tr><td>0001b</td><td>1.5 KBytes</td></tr><tr><td>0010b</td><td>1 KBytes</td></tr><tr><td>0011b</td><td>0.5 KBytes</td></tr><tr><td>01xxb</td><td>2 KBytes</td></tr><tr><td>10xxb</td><td>2 KBytes</td></tr><tr><td>11xxb</td><td>2 KBytes</td></tr></table></td></tr>
</table>

PHY0TX, PHY0 TX FIFO Control: A=12h, R=00h

<table>
<tr><th>Bit</th><th>Access</th><th>Description</th></tr>
<tr><td>7:0</td><td>R/W</td><td>phy0, channel 1 TX FIFO control.
Tells the bridge how much data needs to be in the phy0 1 txfifo before ixp dtpa[1], ixp ptpa (when channel is selected by ixp tadr[1:0]) and ixp stpa (when channel is being accessed) are deasserted.
The signal transition occurs just as the FIFO reaches the specified limit regardless of where it is in the packet.
<table><tr><td>0000b</td><td>2 KBytes</td></tr><tr><td>0001b</td><td>1.5 KBytes</td></tr><tr><td>0010b</td><td>1 KBytes</td></tr><tr><td>0011b</td><td>0.5 KBytes</td></tr><tr><td>01xxb</td><td>2 KBytes</td></tr><tr><td>10xxb</td><td>2 KBytes</td></tr><tr><td>11xxb</td><td>2 KBytes</td></tr></table></td></tr>
<tr><td>3:0</td><td>R/W</td><td>phy0, channel 0 TX FIFO control.
Tells the bridge how much data needs to be in the phy0 0 txfifo before ixp dtpa[0], ixp ptpa (when channel is selected by ixp tadr[1:0]) and ixp stpa (when channel is being accessed) are deasserted.
The signal transition occurs just as the FIFO reaches the specified limit regardless of where it is in the packet.
<table><tr><td>0000b</td><td>2 KBytes</td></tr><tr><td>0001b</td><td>1.5 KBytes</td></tr><tr><td>0010b</td><td>1 KBytes</td></tr><tr><td>0011b</td><td>0.5 KBytes</td></tr><tr><td>01xxb</td><td>2 KBytes</td></tr><tr><td>10xxb</td><td>2 KBytes</td></tr><tr><td>11xxb</td><td>2 KBytes</td></tr></table></td></tr>
</table>

PHY1TX, PHY1 TX FIFO Control: A=13h, R=00h

Bit	Access	Description
7:0	R/W	phy1, channel 1 TX FIFO control. Tells the bridge how much data needs to be in the phy1 1 txfifo before ixp dtpa[3], ixp ptpa (when channel is selected by ixp tadr[1:0]) and ixp stpa (when channel is being accessed) are deasserted. The signal transition occurs just as the FIFO reaches the specified limit regardless of where it is in the packet. 0000b: 2 KBytes 0001b: 1.5 KBytes 0010b: 1 KBytes 0011b: 0.5 KBytes 01xxb: 2 KBytes 10xxb: 2 KBytes 11xxb: 2 KBytes
3:0	R/W	phy1, channel 0 TX FIFO control. Tells the bridge how much data needs to be in the phy1 0 txfifo before ixp dtpa[2], ixp ptpa (when channel is selected by ixp tadr[1:0]) and ixp stpa (when channel is being accessed) are deasserted. The signal transition occurs just as the FIFO reaches the specified limit regardless of where it is in the packet. 0000b: 2 KBytes 0001b: 1.5 KBytes 0010b: 1 KBytes 0011b: 0.5 KBytes 01xxb: 2 KBytes 10xxb: 2 KBytes 11xxb: 2 KBytes

IXPRX HI CNTR, IXP Receive Counter High: A=15h, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when any rxfifo is unloaded. Note that this counts the number of DWORDs unloaded. This register is the high byte of IXPRX CNTR.

PHY0RX HI CNTR, PHY0 Receive Counter High: A=16h, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when either phy0 0 rxfifo or phy0 1 rxfifo is loaded. Note that this counts the number of DWORDs loaded. This register is the high byte of PHY0RX CNTR.

PHY1RX HI CNTR, PHY1 Receive Counter High: A=17h, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when either phy1 0 rxfifo or phy1 1 rxfifo is loaded. Note that this counts the number of DWORDs loaded. This register is the high byte of PHY1RX CNTR.

IXPRX CNTR, IXP Receive Counter: A=18h, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when any rxfifo is unloaded. Note that this counts the number of DWORDs unloaded.

PHY0RX CNTR, PHY0 Receive Counter: A=19h, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when either phy0 0 rxfifo or phy0 1 rxfifo is loaded. Note that this counts the number of DWORDs loaded.

PHY1RX CNTR, PHY1 Receive Counter: A=1Ah, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when either phy1 0 rxfifo or phy1 1 rxfifo is loaded. Note that this counts the number of DWORDs loaded.

IXPTX CNTR, IXP Transmit Counter: A=1Bh, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when any txfifo is loaded. Note that this counts the number of DWORDs loaded.

PHY0TX CNTR, PHY0 Transmit Counter: A=1Ch, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when either phy0 0 txfifo or phy0 1 txfifo is unloaded. Note that this counts the number of DWORDs unloaded.

PHY1TX CNTR, PHY1 Transmit Counter: A=1Dh, R=00h

Bit	Access	Description
7:0	RO	This is a rolling counter that is incremented when either phy1 0 txfifo or phy1 1 txfifo is unloaded. Note that this counts the number of DWORDs unloaded.

DEBUG0, Debug0: A=1Eh, R=00h

Bit	Access	Description
7	R/W	phy1, channel 1, tx fifo overflow interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
6	R/W	phy1, channel 0, tx fifo overflow interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
5	R/W	phy0, channel 1, tx fifo overflow interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
4	R/W	phy0, channel 0, tx fifo overflow interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
3	R/W	phy1, channel 1, rx fifo overflow interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
2	R/W	phy1, channel 0, rx fifo overflow interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
1	R/W	phy0, channel 1, rx fifo overflow interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
0	R/W	phy0, channel 0, rx fifo overflow interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.

DEBUG1, Debug1: A=1Fh, R=00h

Bit	Access	Description
7	R/W	This bit has no effect on hardware.
6	R/W	PHY loopback When this bit is set to a 1, PHY0 TX is connected to PHY0 RX, and PHY1 TX is connected to PHY1 RX. Should be used for debug purposes only, normally this bit should be clear.
5	R/W	phy1 tprty invert. Invert the outgoing phy1 tprty signal. This will cause a parity error at the receiving device. Should be used for debug purposes only, normally this bit should be clear.
4	R/W	phy0 tprty invert. Invert the outgoing phy0 tprty signal. This will cause a parity error at the receiving device. Should be used for debug purposes only, normally this bit should be clear.
3	R/W	ixp rprty invert. Invert the outgoing ixp rprty signal. This will cause a parity error at the receiving device. Should be used for debug purposes only, normally this bit should be clear.
2	R/W	phy1 rx parity error interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
1	R/W	phy0 rx parity error interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.
0	R/W	ixp tx parity error interrupt debug. An interrupt is sourced when this bit is loaded to a 1. Should be used for debug purposes only, normally this bit should be clear.

Glossary

Access Time A factor in measurement of a memory storage device's operating speed. It is the amount of time required to perform a read operation. More specifically, it is the period of time between which the memory receives a read command signal and the time when the requested data becomes available to the system data bus.

Address A number that identifies the location of a word in memory. Each word in a memory storage device or system has a unique address. Addresses are always specified as a binary number, although octal, hexadecimal, and decimal numbers are often used for convenience.

ANSI (American National Standards Institute) An organization dedicated to advancement of national standards related to product manufacturing.

ATM Asynchronous Transfer Mode.

Bit A binary digit.

Boot The process of starting a computer and loading the operating system from a powered down state (cold boot) or after a computer reset (warm boot). Before the operating system loads, the computer performs a general hardware initialization and resets internal registers.

Boot Device The storage device from which the computer boots the operating system.

BRG Baud Rate Generator.

Byte A group of 8 bits.

CAM Content Addressable Memory.

CAS (Column Address Strobe) An input signal from the DRAM controller to an internal DRAM latch register specifying the column at which to read or write data. The DRAM requires a column address and a row address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of column addresses and row addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

COM Port A bi-directional serial communication port which implements the RS-232 specification.

CPM Communications Processor Module.

CPU (Central Processing Unit) A semiconductor device which performs the processing of data in a computer. The CPU, also referred to as the microprocessor, consists of an arithmetic/logic unit to perform the data processing, and a control unit which provides timing and control signals necessary to execute instructions in a program.

Default The state of all user-changeable hardware and software settings as they are originally configured before any changes are made.

DMA Direct Memory Access.

DRAM	(Dynamic Random Access Memory) Semiconductor RAM memory devices in which the stored data does not remain permanently stored, even with the power applied, unless the data are periodically rewritten into memory during a refresh operation.
Driver	A software component of the operating system which directs the computer interface with a hardware device. The software interface to the driver is standardized such that application software calling the driver requires no specific operational information about the hardware device.
ECC	(Error Checking and Correction) A feature that allows detection of single or multi-bit errors in DRAM reads and correct single bit errors.
EEPROM	(Electrically Erasable Programmable ROM) Specifically, those EPROMs which may be erased electrically as compared to other erasing methods.
External Device	A peripheral or other device connected to the computer from an external location via an interface cable.
FIFO	First In First Out.
Flash Memory	A fast EEPROM semiconductor memory typically used to store firmware such as the computer BIOS. Flash memory also finds general application where a semiconductor non-volatile storage device is required.
FPGA	(Field Programmable Gate Array) A large, general-purpose logic device that is programmed at power-up to perform specific logic functions.
GB or GByte	(Gigabyte) Approximately one billion (US) or one thousand million (Great Britain) bytes. 2^30 = 1,073,741,824 bytes exactly.
GPR	General Purpose Register.
h	(Hexadecimal) A base-16 numbering system using numeric symbols 0 through 9 plus alpha characters A, B, C, D, E, and F as the 16 digit symbols. Digits A through F are equivalent to the decimal values 10 through 15.
Hang	A condition where the system microprocessor suspends processing operations due to an anomaly in the data or an illegal instruction.
Header	A mechanical pin and sleeve style connector on a circuit board. The header may exist in either a male or female configuration. For example, a male header has a number and pattern of pins which corresponds to the number and pattern of sleeves on a female header plug.
Host Bus	The address/data bus that connects the CPU and the chipset.
INT	(Interrupt Request) A software-generated interrupt request.
I/O	(Input/Output) The communication interface between system components and between the system and connected peripherals.
ISR	(Interrupt Service Routine) A program executed by the microprocessor upon receipt of an interrupt request from an I/O device and containing instructions for servicing of the device.
Jumper	A set of male connector pins on a circuit board over which can be placed coupling devices to electrically connect pairs of the pins. By electrically connecting different pins,

	a circuit board can be configured to function in predictable ways to suit different applications.
KB or KByte	(Kilobyte) Approximately one thousand bytes. $2^{10} = 1024$ bytes exactly.
LBA	(Logical Block Addressing) A method the system BIOS uses to reference hard disk data as logical blocks, with each block having a specific location on the disk. LBA differs from the CHS reference method in that the BIOS requires no information relating to disk cylinders, heads, or sectors. LBA can be used only on hard disk drives designed to support it.
LED	Light Emitting Diode.
Logical Address	The memory-mapped location of a segment after application of the address offset to the physical address.
MAC	Media Access Controller.
MB or MByte	(Megabyte) Approximately one million bytes. 2^20 = 1,048,576 bytes exactly.
Memory	A designated system area to which data can be stored and from which data can be retrieved. A typical computer system has more than one memory area.
Memory shadowing	Copying information from an extension ROM into DRAM and accessing it in this alternate memory location.
MMU	Memory Management Unit.
MP	Management Port.
NMI	Non-maskable Interrupt.
NPU	Network Processor Unit.
Offset	The difference in location of memory-mapped data between the physical address and the logical address.
OS	Operating System.
PAL	(Programmable Array Logic) A semiconductor programmable ROM which accepts customized logic gate programming to produce a desired sum-of-products output function.
PCI	(Peripheral Connect Interface) A popular microcomputer bus architecture standard.
Peripheral Device	An external device connected to the system for the purpose of transferring data into or out of the system.
PHY	Physical Interface Layer.
Physical Address	The address or location in memory where data is stored before it is moved as memory remapping occurs. The physical address is that which appears on the computer's address bus when the CPU requests data from a memory address. When remapping occurs, the data can be moved to a different memory location or logical address.
PICMG	PCI Industrial Computer Manufacturer's Group.
Pinout	A diagram or table describing the location and function of pins on an electrical connector.
PLD	Programmable Logic Device.

PLL (Phase-Locked Loop) A semiconductor device which functions as an electronic feedback control system to maintain a closely regulated output frequency from an unregulated input frequency. The typical PLL consists of an internal phase comparator or detector, a low pass filter, and a voltage controlled oscillator which function together to capture and lock onto an input frequency. When locked onto the input frequency, the PLL can maintain a stable, regulated output frequency (within bounds) despite frequency variance at the input.

POST (Power On Self Test) A diagnostic routine which a computer runs at power up. Along with other testing functions, this comprehensive test initializes the system chipset and hardware, resets registers and flags, performs ROM checksums, and checks disk drive devices and the keyboard interface.

PQFP (Plastic Quad Flat Pack) A popular package design for integrated circuits of high complexity.

Program A set of instructions a computer follows to perform specific functions relative to user need or system requirements. In a broad sense, a program is also referred to as a software application, which can actually contain many related, individual programs.

RAM (Random Access Memory) Memory in which the actual physical location of a memory word has no effect on how long it takes to read from or write to that location. In other words, the access time is the same for any address in memory. Most semiconductor memories are RAM.

RAS (Row Address Strobe) An input signal to an internal DRAM latch register specifying the row at which to read or write data. The DRAM requires a row address and a column address to define a memory address. Since both parts of the address are applied at the same DRAM inputs, use of row addresses and column addresses in a multiplexed array allows use of half as many pins to define an address location in a DRAM device as would otherwise be required.

RDRAM RamBus DRAM.

Reflashing The process of replacing a BIOS image, in binary format, in the flash boot device.

Register An area typically inside the microprocessor where data, addresses, instruction codes, and information on the status on various microprocessor operations are stored. Different types of registers store different types of information.

Reset A signal delivered to the microprocessor by the control bus, which causes a halt to internal processing and resets most CPU registers to a prescribed state. The CPU then jumps to a starting address vector to begin the boot process.

RISC Reduced Instruction Set Computer.

ROM (Read Only Memory) A broad class of semiconductor memories designed for applications where the ratio of read operations to write operations is very high. Technically, a ROM can be written to (programmed) only once, and this operation is normally performed at the factory. Thereafter, information can be read from the memory indefinitely.

RS-232 A popular asynchronous bi-directional serial communication protocol. Among other things, the RS-232 standard defines the interface cabling and electrical characteristics, and the pin arrangement for cable connectors.

RTC	(Real Time Clock) Peripheral circuitry on a computer motherboard which provides a nonvolatile time-of-day clock, an alarm, calendar, programmable interrupt, square wave generator, and a small amount of SRAM. In the NY1210, the RTC operates independently of the system PLL which generates the internal system clocks. The RTC is typically receives power from a small battery to retain the current time of day when the computer is powered down.
SCC	Serial Communications Controller.
SDRAM	Synchronous Dynamic Random Access Memory.
Segment	A section or portion of addressable memory serving to hold code, data, stack, or other information allowing more efficient memory usage in a computer system. A segment is the portion of a real mode address which specifies the fixed base address to which the offset is applied.
SERDES	Serializer, Deserializer.
Serial Port	A physical connection with a computer for the purpose of serial data exchange with a peripheral device. The port requires an I/O address, a dedicated IRQ line, and a name to identify the physical connection and establish serial communication between the computer and a connected hardware device. A serial port is often referred to as a COM port.
SO DIMM	(Small Outline Dual Inline Memory Module) A form factor for memory modules that is smaller and denser than SIMMs. Typically used on laptops.
SRAM	(Static Random Access Memory) A semiconductor RAM device in which the data remains permanently stored as long as power is applied, without the need for periodically rewriting the data into memory.
Standoff	A mechanical device, typically constructed of an electrically non-conductive material, used to fasten a circuit board to the bottom, top, or side of a protective enclosure.
Symmetrically Addressable SIMM	A SIMM, the memory content of which is configured as two independent banks. Each 16-bit wide bank contains an equal number of rows and columns and is independently addressable by the CPU via twin row address strobe registers in the DRAM controller.
TB or TByte	(Terabyte) Approximately one thousand billion (US) or one billion (Great Britain) bytes. 2^40 = 1,099,511,627,776 bytes exactly.
Wait State	A period of one or more microprocessor clock pulses during which the CPU suspends processing while waiting for data to be transferred to or from the system data or address buses.

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